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COMPUTER MODELS FOR ELECTRONIC COMPONENTS WITH AND WITHOUT TEMPERATURE EFFECTS

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United States
Naval Postgraduate School

THESIS

COMPUTER MODELS FOR ELECTRONIC COMPONENTS WITH AND WITHOUT TEMPERATURE EFFECTS

by

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Thesis Advisor: S. G. Chan

December 1971

Approved for public release; distribution unlimited.

Computer Models for Electronic Components
with and without Temperature Effects

by

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Lieutenant, Turkish Navy
B.S., Naval Postgraduate School, 1970

Submitted in partial fulfillment of the
requirements for the degree of

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NAVAL POSTGRADUATE SCHOOL
December 1971

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ABSTRACT

Whenever active or passive devices are included in an electronic circuit that is to be analyzed by a computer, appropriate models for these devices must be developed. The majority of the models that have been adapted for analyzing a circuit on a computer have neglected the effect of ambient temperature on the element. Temperature variation has been shown to have hazardous effects on electronic components. This paper deals with the modification of some existing models to include temperature effects and shows the results of such modifications. It is done for six basic electronic components (i.e., resistor, capacitor, inductor, diode, bipolar transistor and field-effect transistor). Suggestions for extension of this work are also included.

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I. INTRODUCTION

A. GENERAL

It is necessary for the electronic design engineer to predict and identify the response of electronic systems to temperature effects caused by the device itself or the environment. Therefore, in the study of semiconductor electronics the desirability of computer simulation becomes readily apparent. The equations describing semiconductor behavior in all states are complex and nonlinear; hence, solution by manual means is difficult even when many simplifying assumptions are made.

B. BACKGROUND

1. Circuit Analysis by Computer

When a computer is used to analyze an electronic circuit, a sufficient amount of information concerning the circuit parameters must be supplied and device terminal relationships in the network equations describing the circuit must be determined. This is not a difficult task for passive components such as resistors and capacitors. Active devices may be described to computer analysis programs in terms of models which mathematically simulate the behavior of the devices. It has become increasingly important to develop accurate models of these devices for computer programs used in design and analysis of such circuits.

Analyzing the networks requires that the derived equations must be in some particular form and their parameters specified properly by the user. The circuit elements used in a network could include lumped resistances, inductances, and capacitances, current and voltage sources (dependent and independent), and active device models (i.e., diodes and transistors).

In the application of the Computer Aided Analysis Programs the need often arises for a circuit element that is not included in the list of standard elements. The necessity of using linear but nonstandard elements (such as small-signal transistors or ideal transformers) arises in many programs. In the case of linear nonstandard elements, general equivalent circuits have often been developed by others; they can be applied to programs.

2. Simulation of Circuits with Active Elements

Active networks contain dependent current and voltage sources or negative resistors. When we attempt to analyze an active circuit by computer we encounter some problems. The first one is to find a set of mathematical equations to relate the current and voltage characteristics of each device. These equations can be obtained by one of two ways; they can be derived from mathematical description of the physical phenomena occurring during the operation of the device or might be obtained by empirical observations of the behavior of actual device. The degree of the

prediction, over a wide range of operation about actual behavior of the device, determines the value of these equations. Secondly the parameters in these equations must be known or measurable or the required information should be derivable from terminal measurements. The other factor is the tolerance of the parameters.

II. DEVICE-MODELLING METHODS

A. INTRODUCTION

The objective of modelling is to proceed from the fundamentals, that is, from material properties and morphology of a distributed device to a model as presented below:

(1) To obtain systematically a lumped, network-like model for a distributed device, a) one should write equations which are distributed analogs to one of Kirchhoff's two network laws, the current-node law or the voltage-loop law. Since the desired model is network-like, it must obey the two laws of Kirchhoff. b) One should remove, by some method of approximation, all aspects of the mathematical description which can be traced to the distributed nature of the device.

(2) To obtain models which describe the transient performance of a device, one might take advantage of, if possible, knowledge of its steady-state properties. The reason for this is, of course, that many aspects of steady-state behavior are much easier to determine than their transient counterparts.

In practice, a model is rarely perfect. Thus we should search for a model whose elements provide the best combination of linearity and frequency independence.

In this section the four basic approaches will be presented for developing equivalent circuits for elements that are not standard in computer programs. These approaches can be used individually or can be combined to form more complicated device model.

B. PIECEWISE LINEAR MODELLING

In piecewise linear modelling technique nonlinear elements can be analyzed by replacing all the nonlinear components with equivalent circuits, constructed with the linear elements recognized by the computer program. The nonlinear characteristics are averaged over the range of interest and represented approximately by linearized characteristics. For devices passing from one operating region to another (such as a transistor moving from the active region to saturation), a different, linearized equivalent circuit can be proposed for each region.

C. MATHEMATICAL MODELLING

Those circuit elements that are not standard (defined as a circuit element that is not included in the list of built-in models of any computer library) can be modelled using only the mathematical relationship which describes their terminal characteristics. The procedure to follow in developing equivalent circuits using mathematical modelling technique is quite straightforward. In many cases, the modelling problem can be reduced to the synthesis of

a simple RLC network sometimes requiring the use of dependent current sources. In other cases, a little inventiveness is useful.

The equations describing the components must be linear since only linear elements are used in the development of the model. The availability of R, L, and C elements in the construction of the equivalent circuit permits the modelling of linear differential equations with constant coefficients.

D. PHYSICAL ANALOGY: PIECEWISE LINEAR MODELLING

The modelling of a nonlinear element with an algebraic voltage-current relationship (such as nonlinear resistance) was discussed in Section B. In this section the techniques for modelling a nonlinear reactive element with a non-algebraic voltage-current relationship is discussed (such as inductance or capacitance). For better understanding one may refer to examples given in Ref. 17. Since nonlinear inductance and capacitance are algebraic functions of magnetic flux and charge, respectively, which are not recognized by the program, a reasonable solution to this modelling problem is to find a physical analogy which will allow flux or charge to be treated in those units recognized by the program.

The physical analogy acts as a black box which converts the physical relationship into terms which are acceptable to the program as shown in following algorithm. Therefore,

elements such as nonlinear inductances and capacitances can

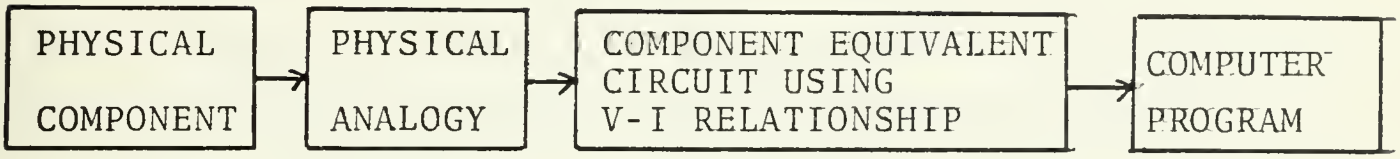

Figure 2-1. Physical Analogy Concept Use in Physical Component Modelling.

be modelled if an analogy between the characteristics to be modelled and a voltage-current relationship acceptable to program can be established.

E. PHYSICAL ANALOGY: MATHEMATICAL MODELLING

Almost all of the Computer Aided Circuit Analysis Programs perform calculations in terms of voltages and currents only. The parameters, such as charge and magnetic flux, have not been included in the programs and cannot be used directly. If such conditions exist, it is necessary to develop methods for expressing the new parameters (charge, magnetic flux, etc.) as functions of voltage and current or to redefine some new elements in addition to the elements included in the standard list that will perform the required analysis in terms of voltage and current.

The solution of mechanical and thermal problems by electrical analogy techniques is an example of this kind. Establishing the analogy is the first step in the derivation of an equivalent circuit. The second step is linking the derived analog network to the remainder of the model which includes the element terminals. The element terminal

characteristic must always be defined in terms of voltage and current. The charge-control transistor model is a good example of physical analogy techniques in modelling the other charge equations which govern the transistor response. See Ref. 17, Appendix A.2.

III. TEMPERATURE EFFECTS

A. TEMPERATURE EFFECTS ON RESISTOR

The resistivity ρ of a conductor is the ratio of the electric intensity E to the current per unit cross-sectional area.

$$\rho = E/(I/A) \qquad 3.1$$

The resistivity of all conducting material is affected by its temperature. A plot of resistivity versus temperature, for a metallic conductor, is given in Fig. 3.1. The curve may be satisfactorily represented by an equation of the form

$$\rho = \rho_0 + g_1 T + g_2 T^2 + g_3 T^3 + \ldots\ldots \qquad 3.2$$

where ρ_0 is the resistivity at 0° C, g_1, g_2, ..., are constants depend on the characteristic of a particular material.

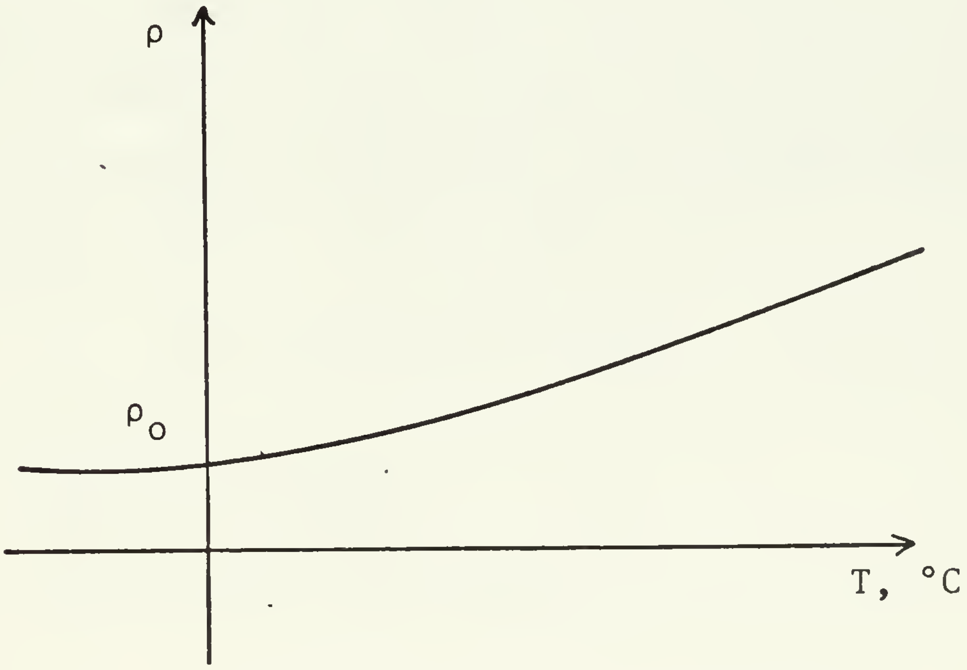

Figure 3-1. Resistivity versus Temperature

For temperatures which are not too great the terms in T^2 and higher powers may be neglected and can be written as

$$\rho = \rho_0 + g_1 T \; . \qquad 3.3$$

The temperature coefficient definition of resistivity is

$$a = g_1/\rho_0 = (\rho-\rho_0)/(\rho_0 T) \qquad 3.4$$

Since the resistance of a given conductor is proportional to its resistivity the following equation can be written

$$R = R_0(1 + aT) \qquad 3.5$$

where R_0 is the resistance at 0° C and R is the resistance at T° C.

The resistivities of nonmetals decrease with increasing temperature, and their a's are negative. Electrolytes also have negative a's.

B. TEMPERATURE EFFECTS ON INDUCTOR

Temperature variation is usually accompanied by a change in inductance, resistance and self-capacitance of a coil. The last two types of change are not important in comparison with the change in inductance. The formula for single-layer solenoid given by Sturley [Ref. 6] is

$$L = (r^2 N^2)/(9r + 10\ell) \qquad 3.6$$

where ℓ = length of winding

r = radius of winding

N = total turns in the coil.

The change of the inductance for an increase in temperature of T° C can be shown to be [Ref. 6]

$$\Delta L = bL(\Delta T) \qquad 3.7$$

where ΔL = change in inductance

b = coefficient of linear expansion of the conductor

ΔT = change in temperature.

Equation 3.7 is valid when the coefficients of radial and axial expansion, b_r and b_ℓ, are approximately equal.

It is possible to make the inductance L independent of temperature by satisfying Eq. 3.8, the ratio of axial to radial expansion.

$$b_\ell/b_r = 2 + (9r/10\ell) \qquad 3.8$$

By choosing the coil-former and the conductor material properly, the temperature coefficient for inductors can be minimized.

C. TEMPERATURE EFFECTS ON CAPACITOR

Temperature variation has two effects on capacitors, namely to change the dielectric permittivity and the disposition of the plates. Some typical capacitance-temperature coefficients will be given in Chapter IV. Permittivity of the insulating material is considerably changed with temperature. Capacitances for parallel plate and cylindrical types are given with the following equations,

$$\text{parallel plate:} \quad C = (A.\varepsilon)/d \qquad 3.9$$

cylindrical: $C = (2\pi . \ell . \varepsilon)/\text{Log}(a/b)$ 3.10

where area of plate (A), and length of capacitor (ℓ), are temperature dependent also, but this dependence can be negligible when compared with the dependence of permittivity. In both cases capacitances are the function of permittivity ε. In addition to temperature dependence of ε, it is dependent of frequency, but the latter effect is a different story.

Improvement of the manufacturing techniques minimizes the temperature coefficient for capacitors.

D. TEMPERATURE EFFECTS ON DIODE

1. Introduction

There are two kinds of charge-carrying particles; one is negative (the free electron) of mobility μ_n, and the other is positive (the hole) of mobility μ_p. These particles move in opposite directions in an electric field E, but since they are of opposite sign, the currents are in the same direction. Hence the current density J is given by

$$J = (n\mu_n + p\mu_p)\, e\, E$$

where n = magnitude of free-electron concentration

p = magnitude of hole concentration

e = electron charge in coulombs.

For an intrinsic semiconductor $n = p = n_i$, where n_i is the intrinsic carrier concentration. The intrinsic carrier concentration n_i is temperature dependent, such as

$$n_i^2 = AT^3 \exp(-E_{GO}/kT) .$$

It has been shown experimentally that E_G depends upon temperature also as pointed out below

$$E_G = E_{GO} - qT$$

where E_{GO} is the energy gap of the semiconductor at 0° K and q is a constant ($q = 2.4 \times 10^{-4}$ eV/°K for silicon and $q = 3.9 \times 10^{-4}$ eV/°K for germanium).* Such a large change in conductivity with temperature places a limitation upon the use of semiconductor devices in some circuits.

2. Temperature Dependence of Parameters

For a p-n junction the current I is related to the voltage V by the equation

$$I = I_o[\exp(V/mV_T)-1] \qquad 3.11$$

Temperature dependent parameters of the Eq. 3.11 are I_o and V_T.

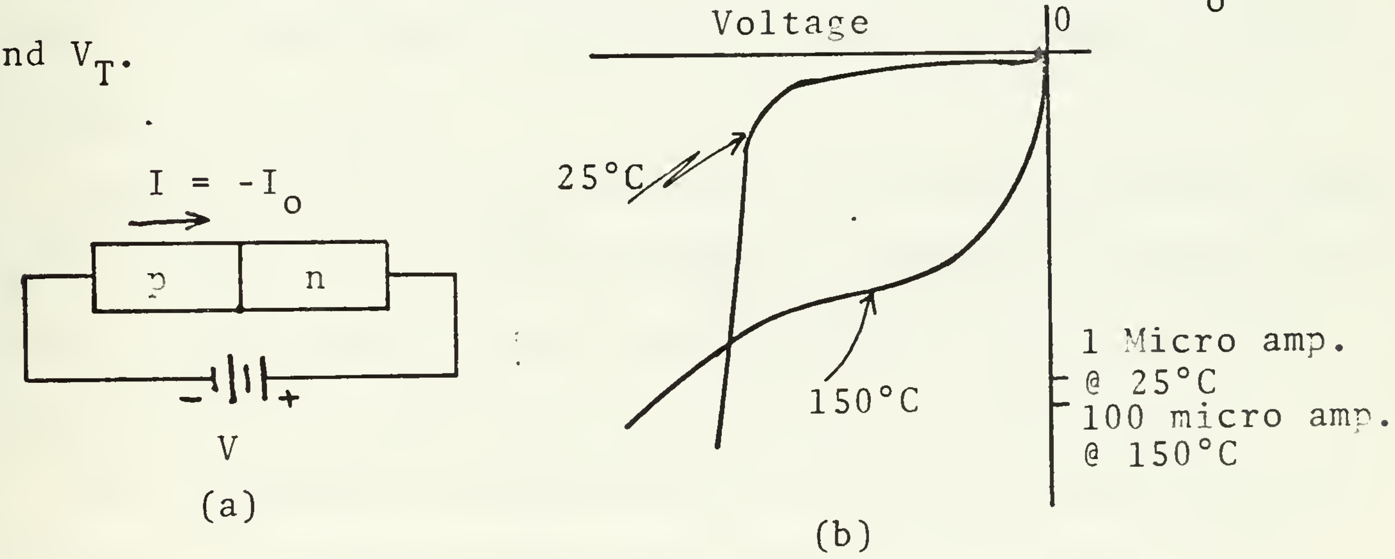

Figure 3-2. Typical Reverse Biased Diode (a), and its Characteristics (b)

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*Strictly speaking, q is not a constant. For example, for silicon $q = 2.4 \times 10^{-4}$ eV/°K only when $T \geq 200°$ K. For germanium, $q = 3.9 \times 10^{-4}$ eV/°K only when $T \geq 150°$ K.

I_o is called the reverse saturation current and given by the equation

$$I_o = K\ T^n \exp(-V_{GO}/mV_T) \qquad 3.11.a$$

for Germanium: $m = 1$ $\quad n = 2$ $\quad V_{GO} = 0.785$ volts

for Silicon: $m = 2$ $\quad n = 1.5$ $\quad V_{GO} = 1.21$ volts

From experimental data we find that the reverse saturation current increases approximately seven per cent per ° C. Since $(1.07)^{10} \cong 2.0$ reverse saturation current approximately doubles for every 10° C rise in temperature. V_T is the "volt equivalent of temperature" defined by

$$V_T = T/11600\ .$$

Another important parameter for diode is diffusion or storage capacitance and given by

$$C_D = \tau\ I/m\ V_T \qquad 3.12$$

where τ is the diode time constant equals the mean lifetime of minority carriers.

Reverse leakage resistance also has some temperature dependence; since it can change depending on the manufacturing process, no generalized temperature coefficient can be stated. It should be determined for each family of the diode.

The temperature coefficient of the diode parameters can be derived in differential form from Eqs. 3.11 and 3.11.a by taking the derivatives and making some approximations to yield the following equations:

$$(1/I_o)(dI_o/dT) = (m/T) + (V_{GO}/mTV_T) \qquad 3.13$$

$$dV/dT = [V-(V_{GO} + nmV_T)]/T \qquad 3.14$$

at fixed current.

E. TEMPERATURE EFFECTS ON TRANSISTOR

1. Introduction

A junction transistor consists of a silicon or germanium crystal, in which a layer of n-type or p-type material sandwiched between two layers of p-type or n-type material, is called a p-n-p or n-p-n transistor. For a qualitative understanding of the form of the input and output characteristics, one can consider that the transistor consists of two diodes placed in series "back to back." It has four operating regions defined as follows:

Region (a): Cut-off region (emitter reverse biased, collector reverse biased),

Region (b): Normal transistor operation (emitter forward biased, collector reverse biased),

Region (c): Saturation region (emitter forward biased, collector forward biased),

Region (d): Inverse transistor operation (emitter reverse biased, collector forward biased). The input-output characteristics of the transistor in different modes are given in many texts.

2. Temperature Dependence of Parameters:

All of the parameters of interest in computer application concerning transistors change with temperature. Some of them are very sensitive to temperature changes, while others may be assumed essentially constant in the analysis. The most temperature sensitive parameters are saturation currents, I_{ES} and I_{CS}, current gain factors, α_N and α_I, and leakage resistances, R_E and R_C. Parameters like time constants, τ_N, τ_I, capacitances C_C, C_E, proportionalities, m_E, m_C, change only slightly over the temperature region of interest as high as 125° C.

(a) Reverse saturation currents: The emitter junction diode saturation current I_{ES} and collector junction diode saturation current I_{CS} are the most temperature sensitive parameters. Suppose that the reverse saturation current at room temperature (300° K) is given by Eq. 3.11.a; it can be written at temperature T + ΔT, as follows:

$$I_{CO} = K_1 T^n \exp(-E_{GO}/kT)$$

$$I_{COT} = K_1(T + \Delta T)^n \exp[-E_{GO}/k(T + \Delta T)] \qquad 3.15$$

equivalently

$$I_{EOT} = K_2(T + \Delta T)^n \exp[-E_{GO}/k(T + \Delta T)] \qquad 3.16$$

Assuming ΔT << T and expanding the Eq. 3.15 in Taylor series, the following can be obtained:

$$I_{COT} = I_{CO}\{1 + [(E_{GO}/kT) + m]\ (\Delta T/T)\} = I_{CO}[1 + \lambda(\Delta T)] \qquad 3.17$$

After numerical substitution it turns out to be

$$I_{COT} \cong I_{CO}(1 + 0.157\ \Delta T)$$

where $\lambda = 0.157/°C$ and is defined as the temperature coefficient for silicon transistor. For greater accuracy, over larger temperature ranges, the equation including the exponential factor directly should be used.

(b) Current gain factors: The current gain factors in normal and inverse modes for common base configuration are given below:

$$\alpha_N = h_{FE}/(1 + h_{FE}) \quad \text{and} \quad \alpha_I = h_{FEI}/(1 + h_{FEI})$$

where h_{FE} is normal mode, common emitter current gain, and h_{FEI} is inverse mode, common emitter current gain. α_N and α_I do not change appreciably with temperature but $(1-\alpha_N)$ or $(1-\alpha_I)$ plays an important role in the following formulas:

$$h_{FE} = \alpha_N/(1-\alpha_N) \quad \text{and} \quad h_{FEI} = \alpha_I/(1-\alpha_I)\ .$$

For example, the variation of common-emitter current gain h_{FE}, with temperature normalized to unity at T - 25° C for the 2N524 transistor is shown in Fig. 3.3.

(c) Reverse leakage resistance: Reverse leakage resistance is temperature dependent to some extent. No generalized temperature coefficient can be stated since it varies, depending upon the process of manufacturing. Therefore, it should be determined for each family of transistor.

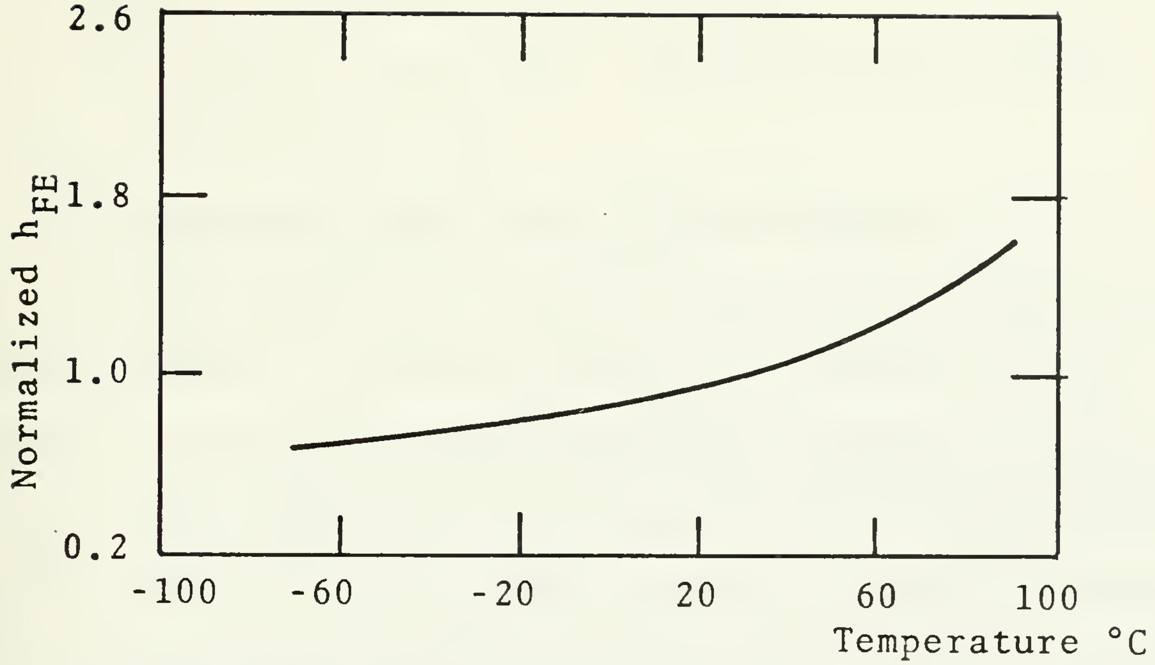

Figure 3-3. h_{FE} versus Temperature

F. TEMPERATURE EFFECTS ON FIELD-EFFECT TRANSISTOR

1. Introduction

Field-effect transistor (FET) has two primary operating regions, namely the triode region in which the device behaves as a voltage-variable resistor, and the pinch-off region where the current is determined mainly by the gate voltage. The two regions are separated by the locus of pinch-off points, i.e., the points where $V_{DS} = V_p - V_{GS}$. V_{DS}, V_P and V_{GS} are defined drain to source voltage, pinch-off voltage and gate to source voltage, respectively.

The operation of FET depends upon the flow of majority carriers only. Therefore, it is a unipolar device. Since

the majority-carrier current decreases with temperature, the troublesome phenomenon [Ref. 4] is not encountered with field-effect transistors. This property provides thermal stability for FET.

2. Temperature Dependence of Parameters

Drain saturation current, I_{DSS} which depends upon channel geometry, impurity density and charge carrier mobility, is defined to be the channel current, I_{DS}, at $V_{GS} = -V_P$. Although I_{DSS} is not greatly dependent on V_{DS}, it depends on temperature heavily. Temperature can influence the drain current in two ways. Firstly, a change in mobility causes a change in resistance of channel. Secondly, a change in temperature causes a change in surface potential. The change in surface potential works in opposition to the change in mobility. Thus, change in surface potential constitutes a built-in gate-voltage compensation of the mobility change in the semiconductor. The effect is dependent on the D.C. gate bias so that at a particular bias the compensation may be optimized.

Another quantity of interest is the transconductance. The transconductance, g_m, has the same temperature variation as I_{DS} does. The principal reason for the negative temperature coefficient of I_{DS} is that the mobility decreases with increasing temperature.

As pointed out before, the major effects of temperature on a FET or alteration of the average channel conductivity

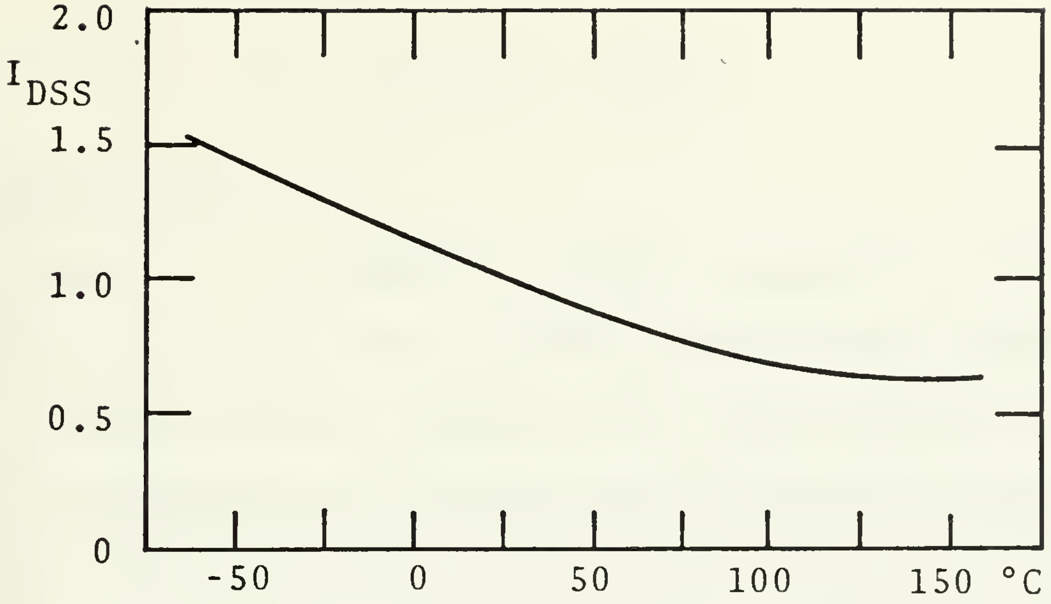

Figure 3-4. Normalized I_{DSS} versus Temperature, at 25° C

and the gate-channel junction barrier potential. Since conductivity decreases with increasing temperature, the drain current decreases as the temperature rises. On the other hand, barrier potential decreases with increasing temperature, causing the magnitude of the total gate-source potential to be reduced, hence increasing the drain current. By suitably choosing the operating point, it is possible to make these effects canceled, producing what is essentially a zero temperature coefficient operating point.

IV. COMPUTER MODELS

A. INTRODUCTION

Almost all the computer analysis programs are designed to solve the linear and nonlinear simultaneous equations which characterize the mathematical models used to predict circuit response for an electrical/temperature environment. The user codes the problem by entering the circuit topology and parameters. Programs contain a standard (built-in) component model library. Non-standard models may be constructed by using standard models. FORTRAN algebraic equations and control statements may be coded to modify standard model parameters, augment the standard models, create nonstandard models, create additional time functions, temperature functions, etc. The circuit is entered into the computer program by using the program standard part models and specifying the circuit topology.

In this paper by "conventional (or non-standard) model," it means the model of a device which is isolated from all environmental effects, and by "modified model," it means a model with temperature effects taken into account. In addition to this task, some additions or some simplifications will be done when necessary, depending upon device characteristics.

In order that electronic components may be handled quantitatively, a set of mathematical relationships must be

derived relating their terminal characteristics. Derivations will not be attempted in this paper since they are documented elsewhere [Refs. 2, 3, 4, 7, 18, 22]; only the results will be presented.

B. RESISTOR MODEL

1. Conventional Model

The resistor model is defined by the following current equation

$$i_R = V_R/R$$

where V_R is the instantaneous voltage across the resistor R.

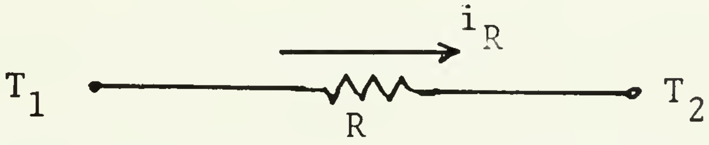

Figure 4-1. Resistor Element

Since the element is bilateral, the choice of which is considered to be terminal 1 and which is terminal 2 depends on the direction of current flow (from T_1 to T_2). This element has just one parameter: the resistance value R.

2. Modified Model

Temperature dependence of resistor was discussed in Chapter III, but the Eq. 3.5 can be rewritten in slightly different form such as

$$R_T = R \pm \Delta R \qquad 4.1$$

where ΔR is the amount of resistance change due to temperature change and equivalent to

$$\Delta R = \pm aR(\Delta T) \qquad 4.2$$

The sign depends on material properties. Assuming resistor is linear, the following modified resistor model for computer can be used. The determination of ΔR requires the parameter a, which can be found in many manuals or reference books.

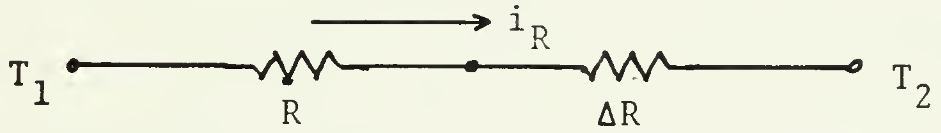

Figure 4-2. Modified Resistor Model

C. CAPACITOR MODEL

1. Conventional Model

A capacitor, shown in Fig. 4.3, is a bilateral element with terminals T_1 and T_2, having a capacitance C. The current flowing through a capacitor is given by

$$i_C = C[d(V_1 - V_2)/dt]$$

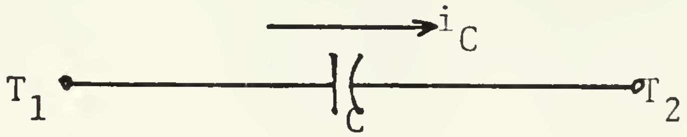

Figure 4-3. Capacitor Element

2. Modified Model

The more realistic capacitor has a shunt leakage resistance and a series resistance as shown below that are identified with R_1 and R_2, respectively.

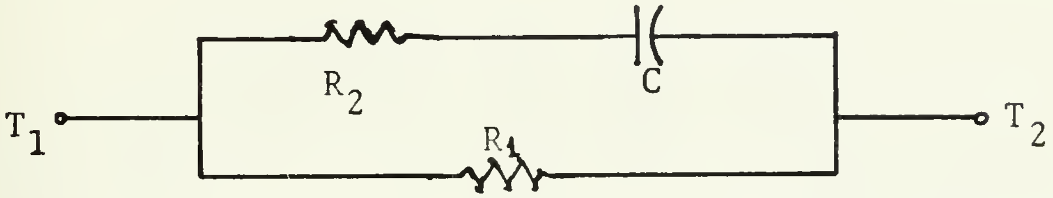

Figure 4-4. Capacitor Model with Resistive Components

Temperature dependence of capacitor was discussed in Chapter III. Very small series resistance (in the order of 0.1 ohms) and very large shunt resistance (in the order of 10^9 ohms) can be assumed constant with temperature change. Some typical capacitance-temperature coefficients are given in the following table and many others can be found in the references given in the footnote.*

Table 4-1. Capacitance-Temperature Coefficients

Insulating Material	Capacitance-Temperature Coefficients
Varnished Cambric	+2100 parts in 10^6 per degree Centigrade
Synthetic Resin	+1600 parts in 10^6 per degree Centigrade
Enamel	+470 parts in 10^6 per degree Centigrade
Ceramic	+100 parts in 10^6 per degree Centigrade

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*(1) Handbook of Chemistry and Physics; (2) International Critical Tables Vol. 2, McGraw-Hill; (3) Tables of Dielectric Materials, Vols. I-IV, MIT, January, 1953.

Defining a change in capacitance as ΔC the modified capacitor model can be obtained shown in Fig. 4-5, in which ΔC should be calculated and added to the model with the aid of tables (given in the footnote on page 30) and the Eqs. 3.9 and 3.10. The change in capacitance is very important if the capacitor is an element of resonance circuit because a small change in capacitance may cause a large drift in resonance frequency.

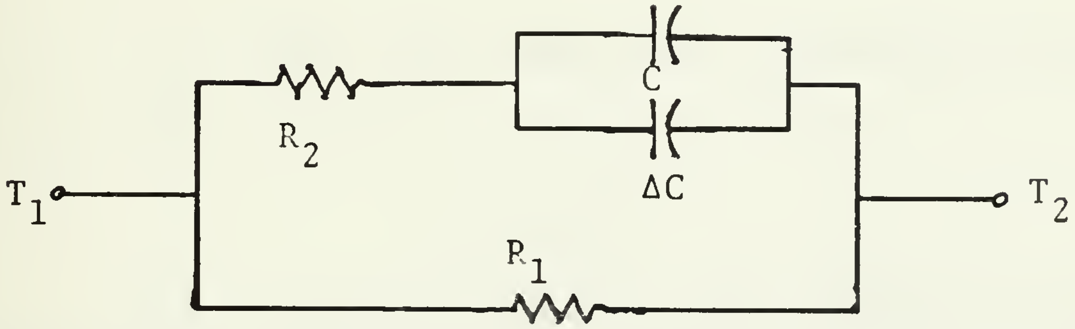


Figure 4-5. Capacitor Model with Temperature Effect

D. INDUCTOR MODEL

1. Conventional Model

The relationship for current is given by

$$i_L = (1/L)\int (V_1 - V_2)\, dt$$

where L is the value of inductance in henries and the difference, $(V_1 - V_2)$, is the voltage across the element. The inductor is diagrammed in Fig. 4-6. Since the inductor is bilateral, the choice of which to be considered T_1 is completely arbitrary. This element has two parameters: inductance L, and Q (of the coil). Many applications of inductors have practical equivalent circuit that also includes the

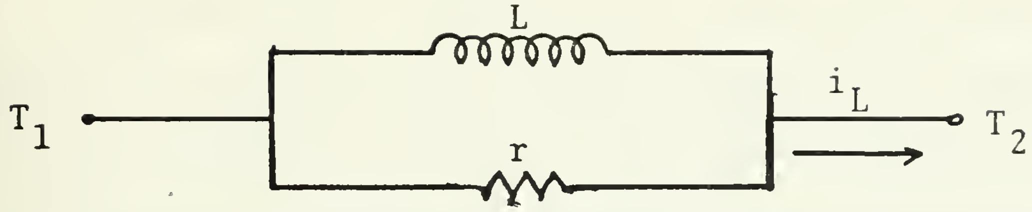


Figure 4-6. Inductor Element

quantity Q--not just pure inductance. Frequency dependent r is given by

$$r = Q.2\pi fL \qquad 4.3$$

where f is the frequency at which the analysis is being performed. The significance of Eq. 4.3 is best seen in a sketch of resistance versus frequency. The range for the Q model is that r becomes unrealistically small as frequency

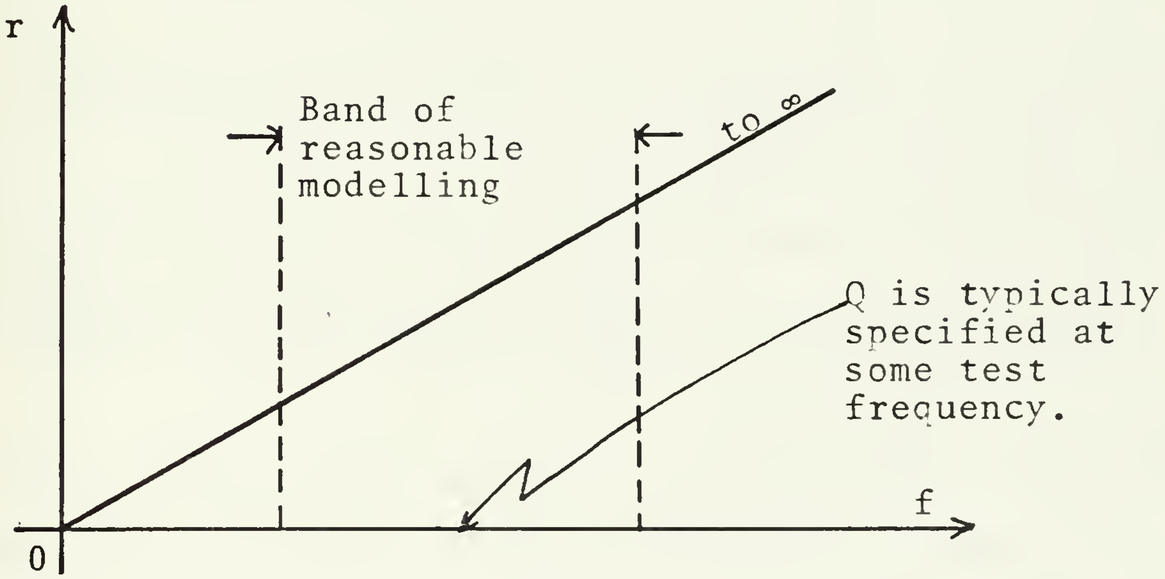


Figure 4-7. Resistance r versus Frequency f

becomes very low, and at high frequency the model would show r approaching infinity which is also unrealistic.

2. Modified Model

Temperature dependence of inductance was given in Chapter III with Eq. 3.7. Additionally D.C. series resistance and the shunt leakage resistance should be involved into the model, which are assumed to be independent of temperature. The schematic which takes all the effects explained above into consideration is shown in Fig. 4.8.

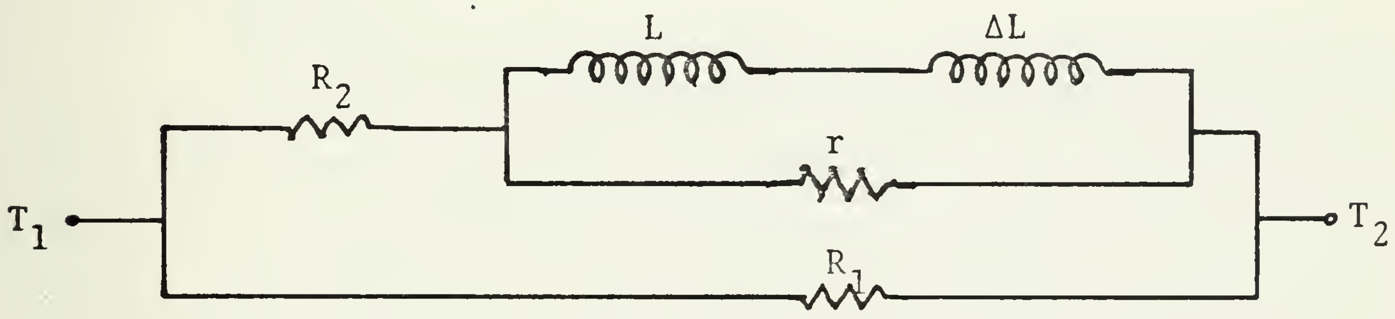


Figure 4-8. Inductor Model with Temperature Effect

To determine ΔL one should first determine the parameter b in Eq. 3.7. The value of b can be found in the handbooks specified in the footnote in previous section. For better understanding of importance ΔL, look at the example given below.

Example: For a tank circuit, $f_o = 1/(2\pi\sqrt{LC})$. If Δf is the change in oscillation frequency due to ΔL change in L, the following relationship can be obtained after proper substitution and expansion by the Binomial Theorem where only the linear term is retained:

$$\frac{\Delta f}{f} = \left(\frac{1}{2}\right)\left(\frac{\Delta L}{L}\right)$$

The value of b for copper is 1.6×10^{-5} parts per ° C. Thus the ratio change in frequency due to the unhindered expansion of a copper coil is 8×10^{-6} parts per ° C, or for $\Delta T = 30°$ C the ratio change of frequency is 240 parts in 10^{6}. Frequency variations due to coil expansion of 240 and 2400 hz at oscillation frequencies of 1 and 10 Mhz, respectively, would be expected under these conditions.

E. DIODE MODEL

1. General

Any diode can be modelled using the following approach. The quantities of interest are electrical characteristics which can be observed at the external terminals (i.e., a "black-box" approach). This type of modelling requires finding a mathematical expression to represent each electrical characteristic. In this paper this method will be emphasized. Physical constants will be used whenever possible, but if a characteristic cannot be related physically, an empirical description will be used.

Based on the operating range, diode models may be classified into two groups: "small-signal" and "large-signal" models. The first type consists of finding an operating point and assuming that all responses are linear about that point. Therefore, this model is valid over only a limited operating range, namely, where the response characteristic is linear. Large-signal model is one which can be used over a wide range of operation. By its nature, it is the best

suited model for use in general computer analysis. There are three most widely known models: (1) Ebers-Moll [Ref. 10], (2) Beaufoy-Sparkes charge-control model [Ref. 11], and (3) Linvill lumped model [Ref. 12]. In this paper Ebers-Moll model will be examined in more detail and necessary modifications will be given. The reason for this preference is this model describes the "black-box" behavior with relatively simple mathematical equations.

2. Model without Temperature Effects

The current equation for diode was given before in Eq. 3.11. Another diode current equation will be obtained by discussing the various factors in the semiconductor diode which have to do with its electrical performance.

With the application of an external reverse bias, the p-n junction width will expand because more donors and acceptors will be uncovered. This increase in uncovered charge with applied voltage may be considered a capacitive effect, named transition-region capacitance.

If bias in the forward direction, the potential barrier at the junction is lowered and holes from the p-side enter into n-side. Similarly, electrons from the n-side move into p-side. A change of voltage on the p-n junction will alter the amount of stored carriers. This, then looks like a capacitor to the accompanying circuit, named storage or diffusion capacitance.

By taking the leakage resistance into account, the following diode current equation can be written as

$$I_D = I + E/R_L + C_D(dE/dt) + C_T(dE/dt) \qquad 4.4$$

These previously derived properties are now all combined to provide a composite equivalent circuit, or computer model, of the p-n junction diode, shown in Fig. 4.9.

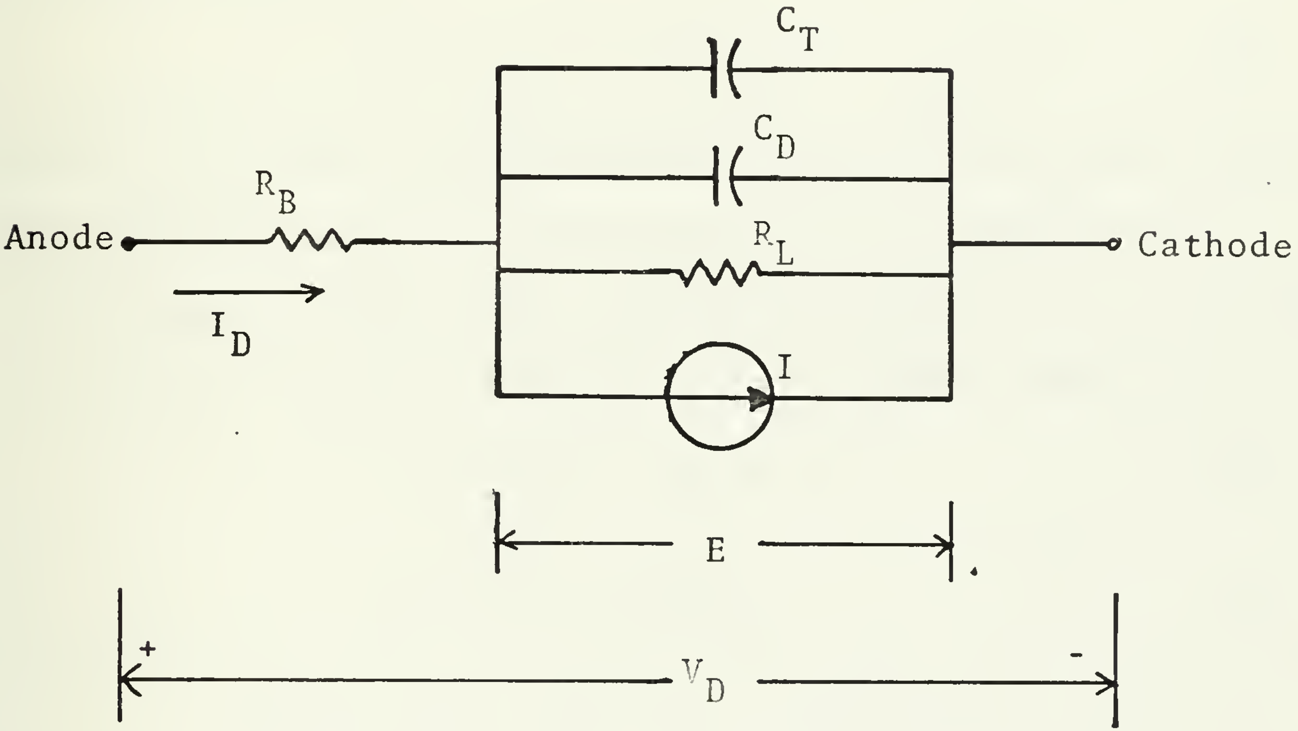


Figure 4-9. Diode Computer Model

The definition and determination of the model parameters will be discussed in the following section.

3. Determination of Model Parameters

Ideal model parameters can be read directly or extracted from the device specification sheet. Unfortunately, this cannot always be done. Most data sheets do not contain sufficient information to define the entire model.

In Fig. 4-9, R_B represents the semiconductor bulk resistance, R_L the junction leakage resistance, C_T the transition capacitance, and I is an ideal current source which describes the forward current as a function of junction voltage E. It is possible to write the Eq. 3.11 in slightly different form as given below:

$$I = I_o[\exp(eE/mkT)-1] \qquad 4.5$$

where e, k, and T are electronic charge, Boltzmann's constant, and absolute junction temperature in °K, respectively. I_o and m are constants which define the shape of the V-I characteristics. For D.C. operation, the network equations are:

$$V_D = E + I_D R_B \qquad 4.6$$

$$I_D = I + E/R_L \qquad 4.7$$

A plot of the static V_D - I_D characteristic for positive I_D is shown in Fig. 4-10. The current is plotted on a logarithmic scale to illustrate that over a wide range in the forward operating region, $V_D \cong E$. For determining the unknown model parameters I_o, m, and R_B one method is to curve-fit data points on the forward diode characteristic to Eqs. 4.6 and 4.7, where I_D is assumed to equal I. Another approach to finding the parameters involves the same assumption but not the curve fitting. One may choose two points on the linear portion of the curve in Fig. 4.10 and label them (I_1, V_1) and (I_2, V_2). In this range may be expressed

with following:

$$I_D = I_o \exp(\theta V_D/m) \qquad 4.8$$

where $\theta = e/kT$.

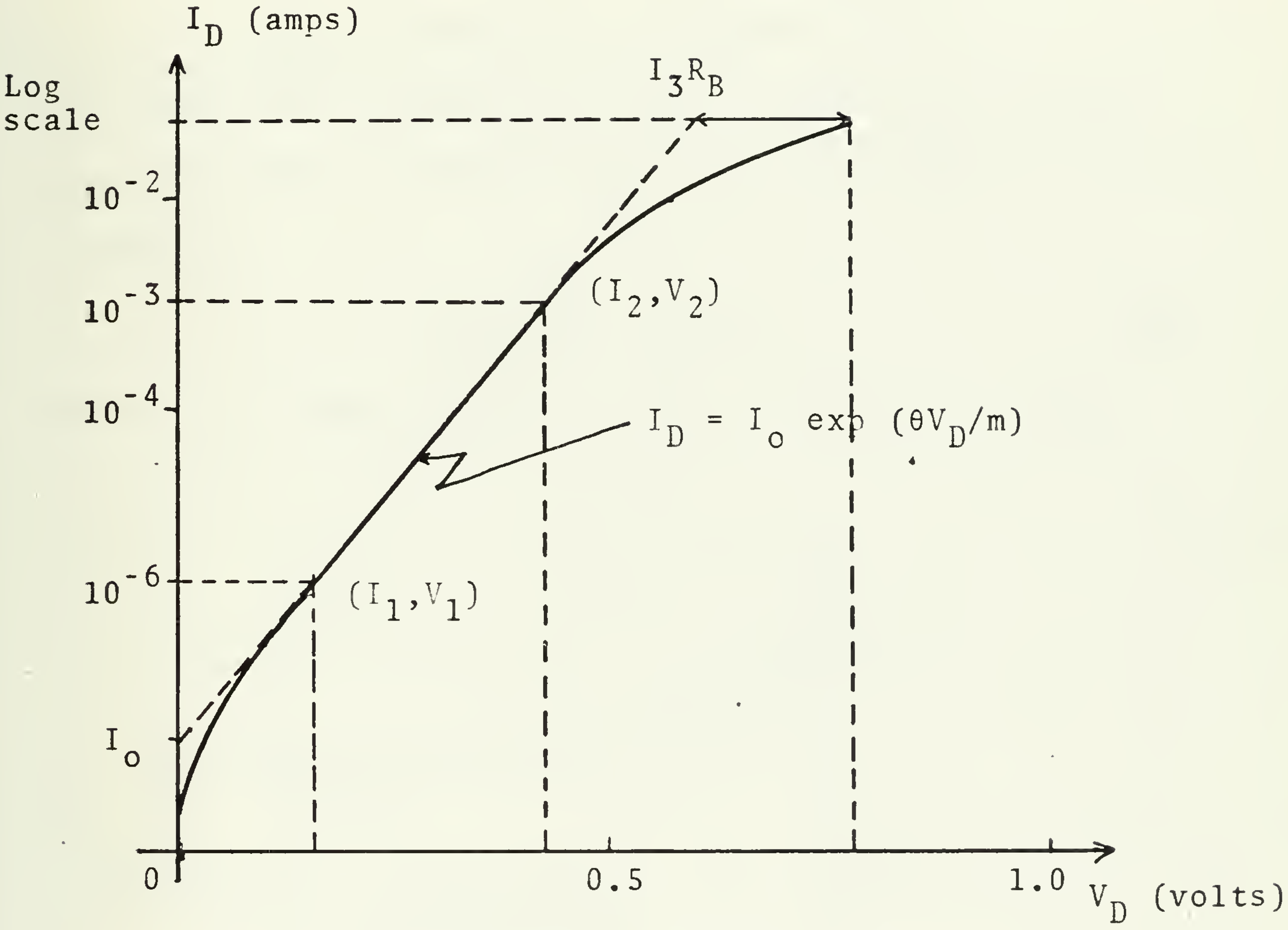


Figure 4-10. Diode Forward V - I Characteristic (Typical)

Taking the logarithm of both sides and substituting (I_1, V_1), (I_2, V_2), then solving for m gives

$$m = \theta(V_2 - V_1)/\ln(I_2/I_1) \quad . \qquad 4.9$$

Substituting either data point and the value of m found in Eq. 4.9 into Eq. 4.8, the following can be obtained:

$$I_o = I_1/\exp(\theta V_1/m) = I_2/\exp(\theta V_2/m) \; .$$

The difference between the linear extrapolation and the measured point is the drop due to R_B. Solution of Eq. 4.6 results in

$$R_B = (V_3 - E_3)/I_3 \qquad 4.10$$

where $E_3 = (m/\theta) \ln [(I_3 + I_o)/I_o] \cong (m/\theta) \ln (I_3/I_o)$.

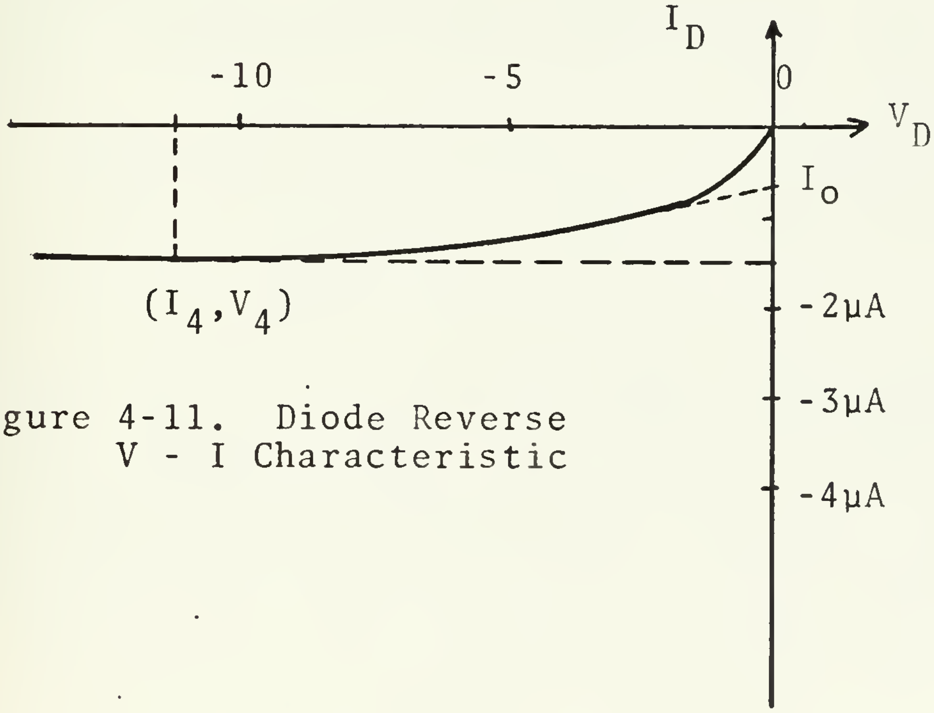


Figure 4-11. Diode Reverse V - I Characteristic

From the reverse characteristic shown in Fig. 4-11, the ohmic leakage resistance, R_L can be found to be

$$R_L = V_4/(I_4 + I_o) \quad . \qquad 4.11$$

There remain two more parameters to be determined, namely, the junction transition capacitance C_T and diffusion capacitance C_D in Fig. 4-9. A typical curve of junction capacitance versus reverse bias is shown in Fig. 4-12.

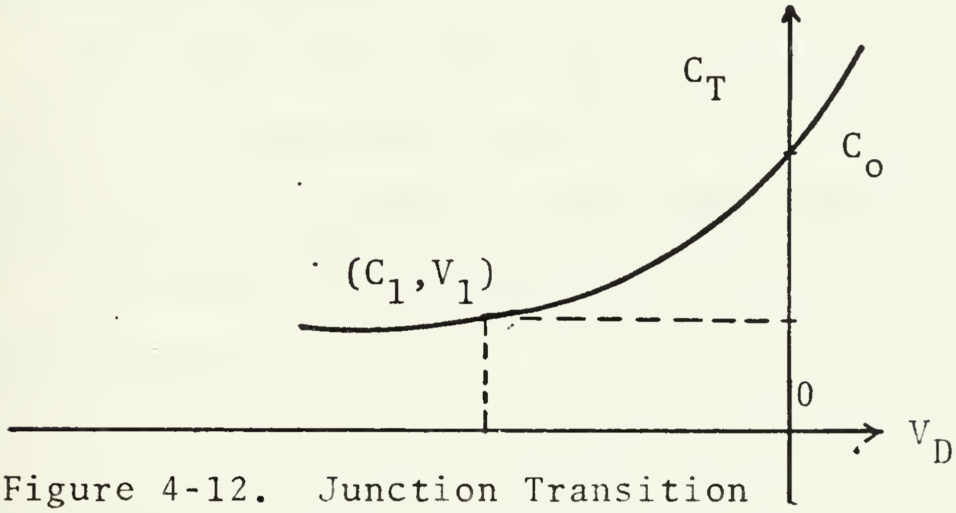


Figure 4-12. Junction Transition Capacitance Characteristic

The analytical expression that describes C_T is

$$C_T = K/(V_J - V_1)^n \qquad 4.12$$

where K, n, and V_J are junction capacitance proportionality constant, grading constant and junction contact potential, respectively (V_J is approximately 0.9 or 1.0 volts). For $V_D = 0.0$, $C_T = C_o = K$. Therefore, at any point (C_1, V_1)

$$C_1 = C_o/(V_J - V_1)^n \quad . \qquad 4.13$$

Solving Eq. 4.13 for n results in

$$n = \ln(C_o/C_1)/\ln(V_J - V_1) \quad . \qquad 4.14$$

Another way of expressing the Eq. 3.12 may be the following:

$$C_D = \theta(I + I_o)/m2\pi f \qquad 4.15$$

where the parameter f is diode cut-off frequency and evaluation of f can be done by Kuno's* method. The cut-off frequency is given by

$$f \cong 1/2\pi\tau \quad .$$

4. Modified Model

The temperature dependence of diode was examined in Chapter III. Temperature coefficient of saturation current and temperature dependence of the diode voltage were given in Eq. 3.13 and 3.14. Equation 4.15 is expressed in more convenient form as

$$C_D \cong \theta I\tau/m = (e\tau/mk)(I/T) \quad . \qquad (4.16)$$

For simplification purposes, making some definitions will be useful at this point such as follows:

$$A = e\tau/mk \qquad 4.17$$

$$B = eE/mk \qquad 4.18$$

C = Fractional increase of reverse current with temperature.

Temperature dependent reverse saturation current increases exponentially as indicated by the following equation:

$$I_{oT} = I_o \exp[C(T - T_o)] \qquad 4.19$$

---

*H. J. Kuno, "Analysis and Characterization of p-n Junction Diode Switching," IEEE Trans. on Electron Devices, Vol. ED-11, p. 8-14, Jan. 1964.

where I_{oT} is the reverse current at temperature T and $I_{o\alpha}$ is the reverse current at temperature T_α. The solution of Eq. 4.19 for C turns out to be

$$C = \ln(I_{oT}/I_{\alpha})/(T - T_{\alpha}) \quad . \qquad 4.20$$

For example 1N3605 silicon diode has the following specifications:

$$\left.\begin{array}{l} I_o = 0.05 \text{ mA at } T_o = 25° \text{ C} \\ I_{oT} = 50 \text{ mA at } T = 150° \text{ C} \end{array}\right\} \text{ Applied Voltage } = -30 \text{ volts.}$$

Therefore

$$C = \ln(50/0.05)/(150 - 25) \cong 0.055/°C \quad .$$

Proceeding with concise form of Eq. 4.16, the following relationship is obtained:

$$C_D = A(I/T) \quad . \qquad 4.21$$

If we drop the unity in the parenthesis in Eq. 4.5 an approximate current equation can be written as

$$I \cong I_o[\exp(eE/mkT)] = I_o \exp(B/T) \qquad 4.22$$

where B is given in Eq. 4.18. The ΔT change in temperature causes the following modification for Eq. 4.22.

$$\begin{aligned} I_T &= I_{oT} \exp[B/(T + \Delta T)] \\ &= I_o \exp(C.\Delta T) \exp[B/(T + \Delta T)] \\ &= I_o \exp(C.\Delta T) \exp(B/T) \exp[-B(\Delta T)/T(T + \Delta T)] \quad . \end{aligned}$$

Definition of another factor such as

$$D = \exp(C.\Delta T) \exp[-B(\Delta T)/T(T + \Delta T)]$$

provides a very short expression for I_T, given below:

$$I_T = D.I \quad . \qquad 4.23$$

On the other hand ΔT change in temperature implies the following modification on diffusion capacitance C_D.

$$\begin{aligned} C_{DT} &= A.I_T/(T + \Delta T) = A.(D.I)/(T + \Delta T) \\ &= (A.I/T)[T.D/(T + \Delta T)] = C_D \; . \; T.D/(T + \Delta T) \\ &= F.C_D \qquad 4.24 \end{aligned}$$

where $F = (T.D)/(T + \Delta T)$. Then adding and substructing the C_D to Eq. 4.24 yields

$$\begin{aligned} C_{DT} &= F.C_D + C_D - C_D \\ &= C_D + C_D\,(F - 1) \; . \qquad 4.25 \end{aligned}$$

In similar fashion

$$\begin{aligned} I_T &= D.I + I - I \\ &= I + I(D - 1) \; . \qquad 4.26 \end{aligned}$$

The temperature treatment of more sensitive diode parameters was given by Eqs. 4.25 and 4.26. The changes due to temperature for R_B and R_L are assumed very small and neglected. Applying all necessary modifications one would get the computer diode model when temperature vatiations exist as shown in Fig. 4-13.

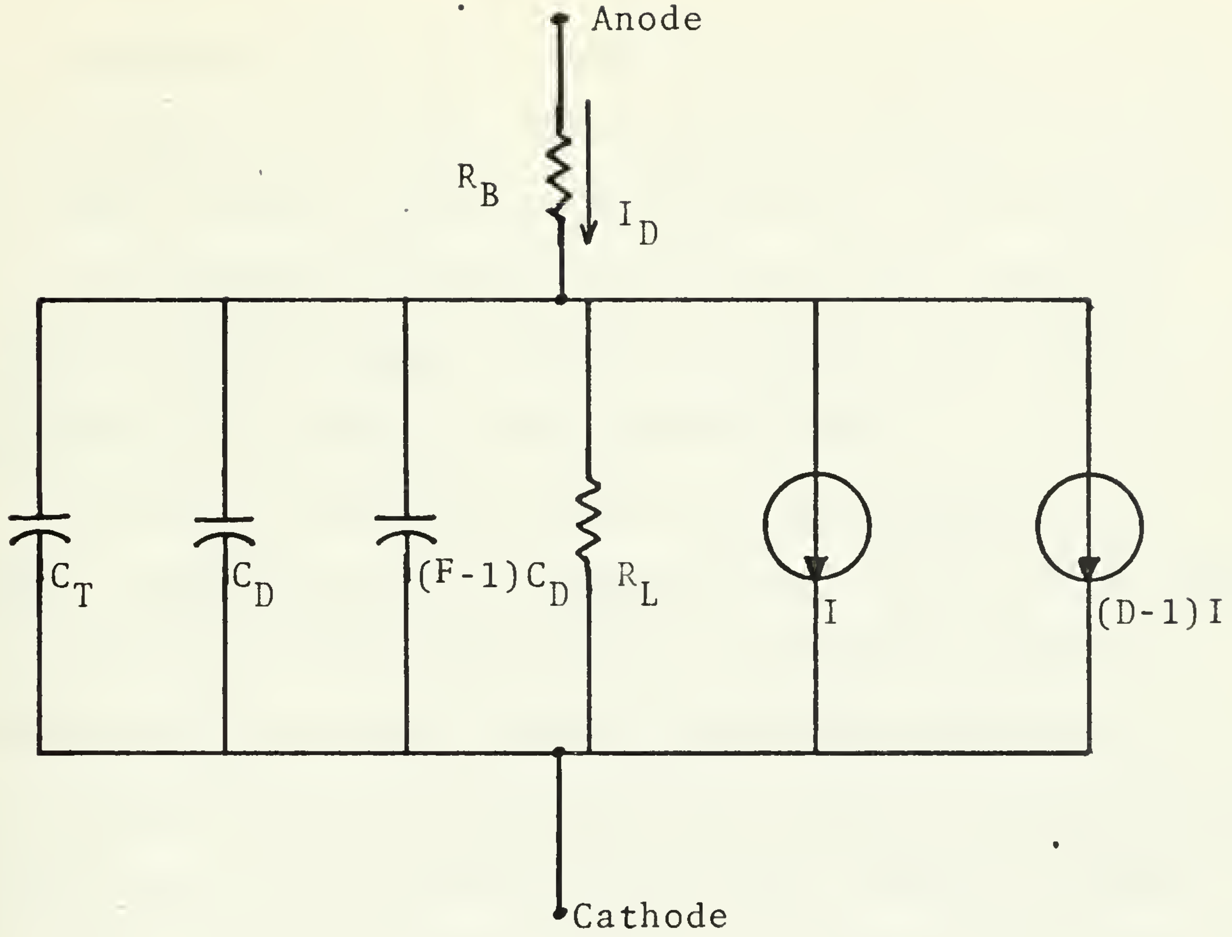


Figure 4-13. Diode Computer Model with Temperature Effects.

F. TRANSISTOR MODEL

1. General

A transistor model in computer-aided analysis should meet the following properties: (a) The model must consist of circuit elements that are recognizable by the computer program being used. (b) The parameters used in the model should either be obtainable from published data or readily estimated. (c) The model should be valid to high frequencies as well as to low frequencies. (d) The model should function without regard to the circuit configuration (common base, common collector, or common emitter) in which the transistor is placed.

Note: A general model for a device does not always lead to the most efficient analysis since certain troublesome elements of the model may not actually be required by the problem at hand. For example, nonlinear or high frequency elements may not affect the circuit response greatly, but could easily affect the solution time significantly.

There are many models that have been proposed to represent transistors at low frequencies. Any of these small-signal models is valid only when the transistor operates in the active region and produces negligible distortion in the output signal. Fortunately the output characteristics of transistors are reasonably linear over a fairly large range, often allowing output swings of several volts with little distortion. High-frequency models for the transistors are more complex than low frequency models, since additional reactive elements are included.

2. Model without Temperature Effect

The transistor is a three-terminal device, fabricated by placing two p-n junctions in close proximity to each other. The current through one forward-biased junction strongly influences the current through the other. The normal mode of transistor operation occurs when the base-emitter junction is a forward biased and base-collector junction is reverse biased. A transistor may also be operated in the inverse mode. In this case, the collector is forward biased and the emitter is reverse biased. Therefore, transistor can be considered as two junction diodes connected in series, of

which one is forward and the other is reverse biased. The emitter junction and the collector junction current equations can be written as in single diode case. By referring to Section E and taking the inverse mode current gain into account, the following current equations may be expressed in terms of diode parameters:

$$I_E = I_{EF} + (V_E/R_{LE}) + C_{TE}(dV_E/dt) + C_{DE}(dV_E/dt) - \alpha_I I_{CF} \quad 4.27$$

$$I_C = I_{CF} + (V_C/R_{LC}) + C_{TC}(dV_C/dt) + C_{DC}(dV_C/dt) - \alpha_N I_{EF} \quad 4.28$$

where parameters α_N and α_I are normal and inverted short-circuit current gains between emitter and collector, capacitors C_{TE} and C_{DE} represent emitter-base depletion-layer and emitter-base diffusion capacitances, respectively. While C_{TC} and C_{DC} represent the collector-base depletion and diffusion capacitances, V_E and V_C are the emitter-base and collector-base voltages, respectively. Emitter and collector reverse saturation currents may be involved into the junction current equations in such a manner given in the following equations:

$$I_{EF} = I_{ES}[\exp(\theta V_E/m_E) - 1] \quad 4.29$$

$$I_{CF} = I_{CS}[\exp(\theta V_C/m_C) - 1] \quad . \quad 4.30$$

I_{ES} and I_{CS} are usually given in specification sheets, but the analytical expressions for I_{ES} and I_{CS} are given as

$$I_{ES} = I_{EO}/(1 - \alpha_N \alpha_I) \quad 4.31$$

and

$$I_{CS} = I_{CO}/(1 - \alpha_N \alpha_I) \quad 4.32$$

where I_{EO} is the saturation current of emitter junction with zero collector current and I_{CO} is the saturation current of collector junction with zero emitter current.

Now we are in a position to model the transistor device. The computer model uses two p-n junctions modelled like the diode previously discussed plus the current gain factors as shown in Fig. 4-14. The resistances R_B and R_C account for ohmic effects and can be approximated as constants in most instances.

The junction capacitance factors are:

Emitter transition capacitance, $C_{TE} = C_{EO}/(V_J - V_E)^n$ 4.33

and

Collector transition capacitance, $C_{TC} = C_{CO}/(V_J - V_C)^n$ 4.34

where n = 1/2 and n = 1/3 for an abrupt junction and a linear graded junction, respectively. C_{EO} and C_{CO} are determined in the same manner as explained in previous section (Section E).

Most transistor manuals give the normal and reverse common emitter current gains $h_{FE(N)}$ and $h_{FE(I)}$. The relationship between the four gain factors is given by

$$\begin{aligned} h_{FE(N)} &= \alpha_N/(1 - \alpha_N) \qquad \alpha_N = h_{FE(N)}/(1 + h_{FE(N)}) \\ h_{FE(I)} &= \alpha_I/(1 - \alpha_I) \qquad \alpha_I = h_{FE(I)}/(1 + h_{FE(I)}) \; . \end{aligned} \tag{4.35}$$

The diffusion capacitances, C_{DE} and C_{DC} are given by

$$C_{DE} = \theta I_{EF} \tau_E/m_E \tag{4.36}$$

and

$$C_{DC} = \theta I_{CF} \tau_C/m_C \tag{4.37}$$

where τ_E and τ_C are emitter and collector time constants, respectively. These time constants can be evaluated by the Kuno's Method that has been mentioned in Section E.

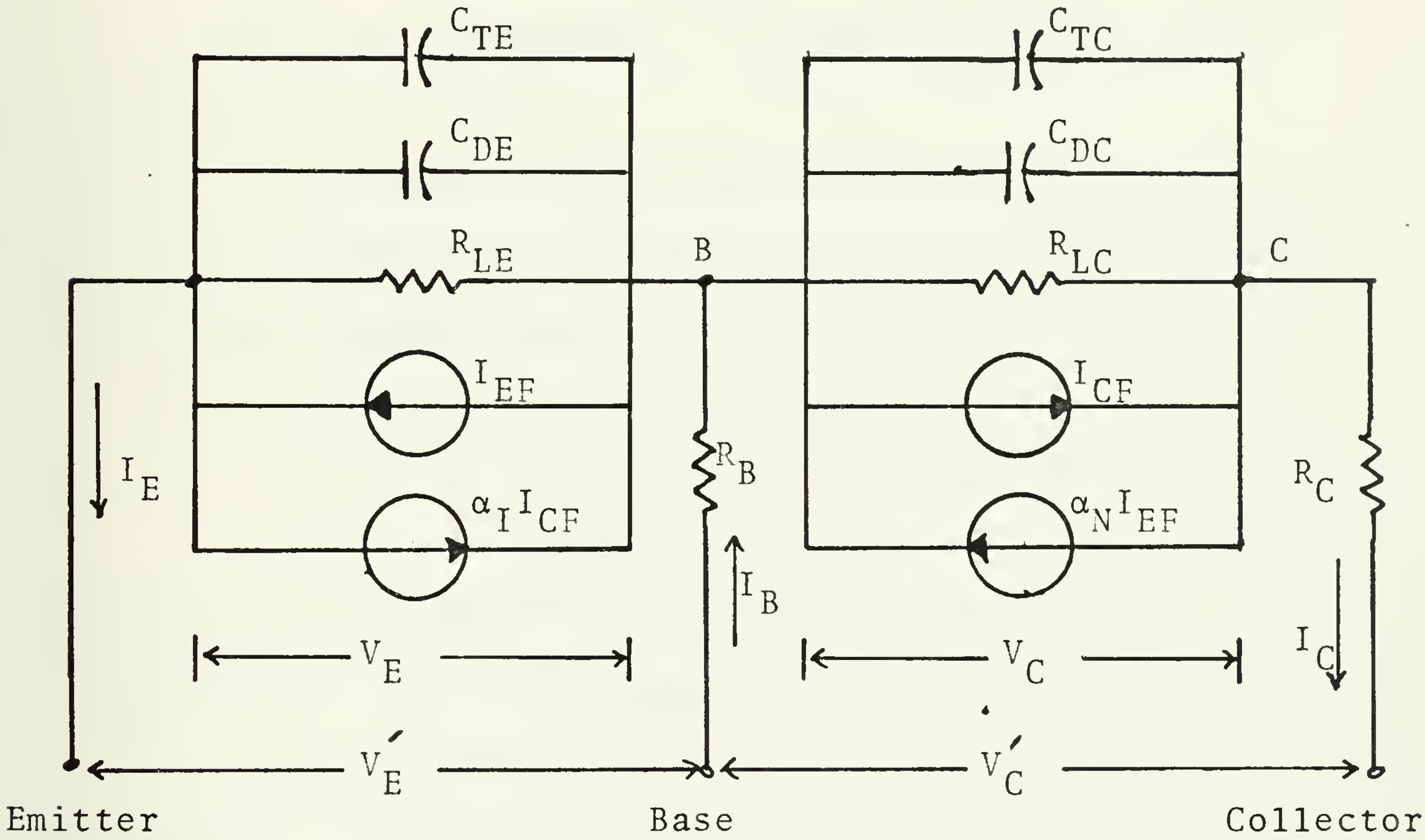


Figure 4-14. n-p-n Transistor Model for Computer Analysis

Most of the transistor parameters are supplied by the manufacturer. However, if it becomes necessary to determine the parameters, Refs. 18, 19, 20 and 21 are very useful for evaluation.

3. Modified Model

The temperature dependence of transistor parameters was discussed and some assumptions were stated in Chapter III. Additional assumptions are given below:

(a) α_N and α_I are approximately the same at temperatures T and $(T + \Delta T)$,

(b) $\Delta T << T$,

(c) τ_E and τ_c are the same at temperatures T and $(T + \Delta T)$,

(d) $I_{EF} \cong I_{ES}[\exp(\theta V_E/m_E)]$ and the same approximation is for I_{CF},

(e) Temperature dependence of R_{LE} and R_{LC} is as explained in Chapter III.

Equation 3.17 was written for collector junction diode saturation current, and a similar expression can be written for emitter jucntion diode saturation current as

$$I_{EOT} = I_{EO}[1 + \lambda_E(\Delta T)]$$

$$= I_{EO} + \lambda_E(\Delta T) \cdot I_{EO} \qquad 4.38$$

where I_{EOT} is emitter junction saturation current at temperature $(T + \Delta T)$ while I_{EO} is at temperature T. The expression for I_{ES} was given by Eq. 4.31 for a specified temperature. If I_{EST} is defined as the value of I_{ES} at temperature $(T + \Delta T)$, the following expression can be written

$$I_{EST} = I_{EOT}/(1 - \alpha_N \alpha_I)$$

$$= [I_{EO} + \lambda_E(\Delta T)\ I_{EO}]/(1 - \alpha_N \alpha_I)$$

$$I_{EST} = I_{EO}/(1 - \alpha_N \alpha_I) + [\lambda_E(\ T) I_{EO}]/(1 - \alpha_N \alpha_I)$$

$$= I_{ES} + K_E\ I_{ES} \qquad 4.39$$

where $K_E = \lambda_E(\Delta T)$. Equation 4.18 was the defining equation for the factor B. A similar definition can be used for emitter junctions as follows:

$$B_E = eV_E/m_E k \quad .$$

For the derivation of I_{EFT}, we first express the term "$\exp[B_E/(T + \Delta T)]$" in a more convenient form as follows:

$$\exp[B_E/(T + \Delta T)] = \exp(B_E/T)\ \exp[-B_E(\Delta T)/T(T + \Delta T)]$$

$$= L_E \exp(B_E/T)$$

where $L_E = \exp[-B_E(\Delta T)/T(T + \Delta T)]$.

Thus for a change in temperature, ΔT , the following approximate expression for the forward emitter current is obtained:

$$I_{EFT} \cong I_{EST}\ [\exp(B_E/T)]L_E$$

$$= (I_{ES} + K_E\ I_{ES})[\exp(B_E/T)]L_E$$

$$= I_{ES}(1 + K_E)L_E \exp(B_E/T)$$

$$= I_{EF}\ (1 + K_E)L_E$$

$$= M_E\ I_{EF} \qquad 4.40$$

where $M_E = L_E(1 + K_E)$.

Another definition given in Section E was Eq. 4.17 which is repeated here for emitter junctions as follows:

$$A_E = e\tau_E/M_E k \quad .$$

Then C_{DE} can be expressed as $C_{DE} = A_E I_{EF}/T$. Therefore, emitter diffusion capacitance at temperature $T + \Delta T$ becomes

$$C_{DET} = A_E\ I_{EFT}/(T + \Delta T)$$

$$= N_E\ C_{DE} \qquad 4.41$$

where $N_E = M_E T/(T + \Delta T)$.

As stated before, a large change in h_{FE}, however, may reflect only a small change in α and in many instances can be neglected in this treatment. Therefore the current generator ($\alpha_N I_{EF}$) in Fig. 4-14, where the temperature variation is not considered, can be written as ($\alpha_N I_{EFT}$) with temperature change (ΔT), so that

$$\alpha_N I_{EFT} = \alpha_N M_E \, I_{EF} \qquad 4.42$$

in which Eq. 4.40 has been applied.

One may follow the same derivations given for the collector junction and obtain the following results:

$$I_{CFT} = M_C \, I_{CF}$$

$$C_{DCT} = N_C \, C_{DC}$$

$$\alpha_I I_{CFT} = \alpha_I M_C \, I_{CF} \quad .$$

Same manipulation can be done for obtaining temperature-caused current generators and capacitors as in the diode case and then the following are obtained:

$$\begin{aligned} I_{EFT} &= M_E \, I_{EF} + I_{EF} - I_{EF} \\ &= I_{EF} + I_{EF} \, (M_E - 1) \\ I_{CFT} &= I_{CF} + I_{CF} \, (M_C - 1) \\ C_{DET} &= N_E \, C_{DE} + C_{DE} - C_{DE} \\ &= C_{DE} + C_{DE} \, (N_E - 1) \\ C_{DCT} &= C_{DC} + C_{DC} \, (N_C - 1) \quad . \end{aligned}$$

Now the modified computer model for transistors can be drawn as shown in Fig. 4-15.

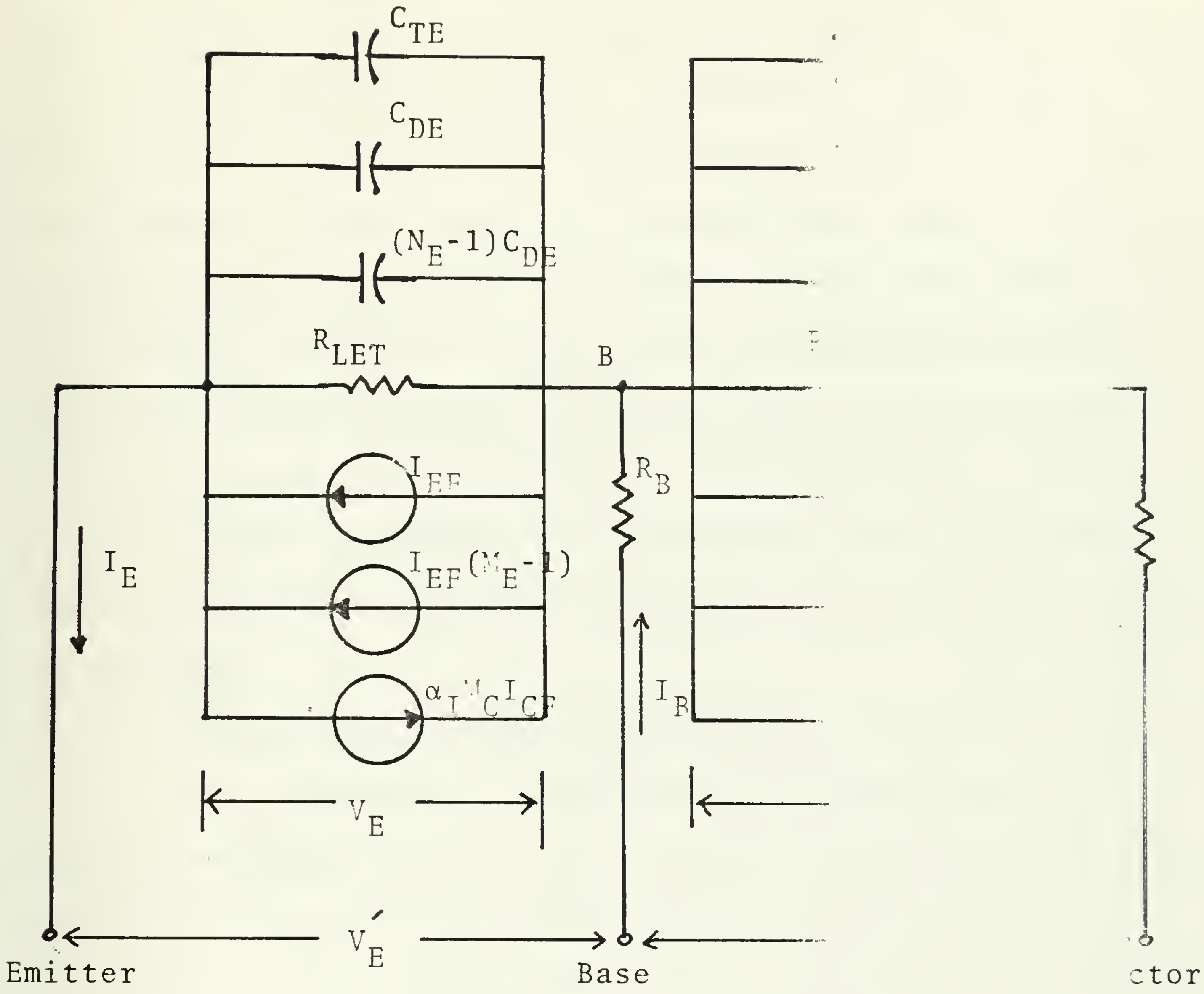


Figure 4-15. n-p-n Temperature Effected T
for Computer Analysis

G. FIELD-EFFECT TRANSISTOR MODEL

1. General

Although field-effect transistors ng used extensively at present, there is no describe all such devices. One reason is al processes causing various modes of operati one another. There are two main types, juncti iated

gate FET, sometimes called the "Metal-Oxide Semiconductor" (MOS) transistor [Ref. 13]. This would suggest the use of at least two different models. A piecewise linear model has been developed by Roberts and Harbourt [Ref. 9] that is designed for circuit analysis using the ECAP [Ref. 1] program. However, piecewise linear models have some deficiencies when applied to general circuit analysis programs because a piecewise linear model can be made to approximate the actual behavior quite accurately by using several regions. However, as more regions are added, more constants must be provided and the awkwardness involved in determining the correct region of operation.

2. Models without Temperature Effects

It is possible to make analogy between vacuum tube (such as a triode) and FET, provided that the cathode is replaced by source, the plate replaced by drain and grid replaced by gate. Neglecting the bulk resistances and taking the barrier capacitances into account, the following equivalent circuit can be obtained. Since the gate junction is

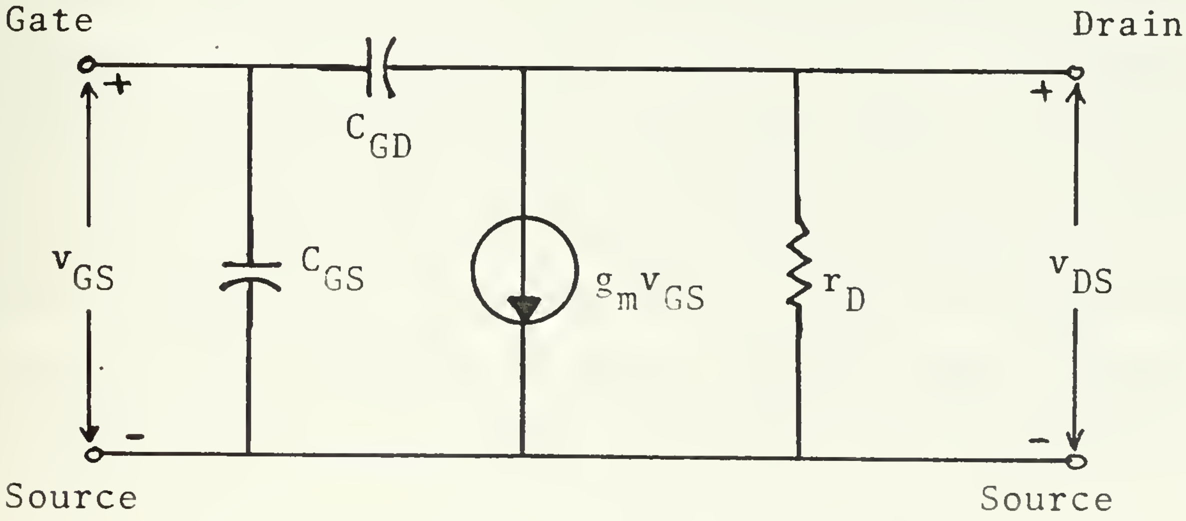


Figure 4-16. Small-Signal JFET Equivalent Circuit

reverse biased, the gate-source resistance r_{GS} and the gate-drain resistance r_{GD} are extremely large, and hence have not been included in the circuit of Fig. 4-16. Determination of the equivalent circuit parameters will be discussed later. As pointed out before there are two categories of field-effect transistors, JFET and MOSFET. As the names imply, a JFET uses the characteristics of a reverse-biased junction to control the drain-source current, while in the MOSFET the gate is a metal deposited on an oxide layer and is insulated from the source and drain. Both devices operate on the principle of a "channel" current controlled by an electronic field. The control mechanisms for the two are different, resulting in considerably different characteristics. The main difference between the two is in the gate characteristics. The input of the JFET behaves like a reverse biased diode while the input of a MOSFET is similar to a small capacitor. Based on the above discussion, the models shown in Figs. 4-17 and 4-18 are obtained.

In Fig. 4-17 the source end of the junction is less strongly reverse-biased or even slightly forward-biased, depending on the instantaneous value of v_{GS}. It exhibits the voltage-variable capacitance and conductance properties of an ordinary p-n diode. A lumped model of this gate-to-source junction can be produced by using the standard built-in model for a junction diode to simulate these effects. Transconductance and output conductance are simulated by the

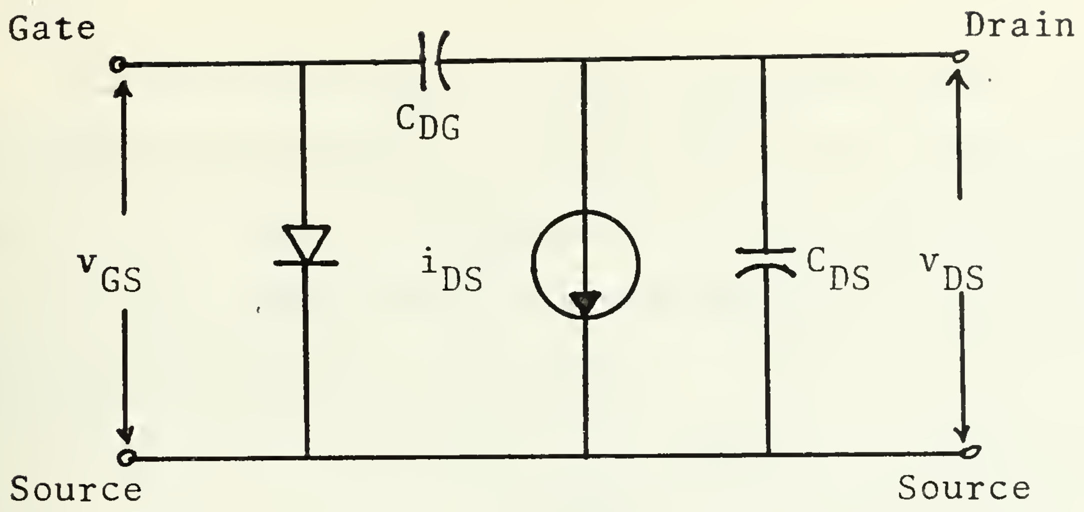


Figure 4-17. Lumped Junction FET Computer Model

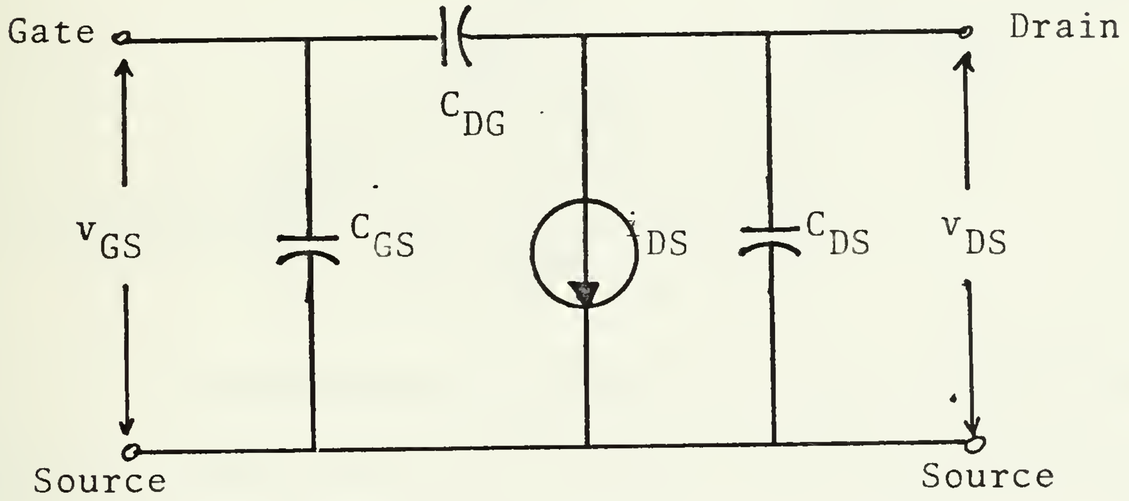


Figure 4-18. Lumped MOSFET Computer Model

nonlinear current source, i_{DS}, which can be modelled by pointwise linearization as described later.

As stated before, the gate of a MOSFET resembles a parallel-plate capacitor with a thin dielectric layer. The dielectric results in a very low gate conductance, and since the thickness is constant, the distributed capacitance is uniform along the channel and independent of v_{GS}. This capacitance can be split between the source and drain ends of the channel and both lumped capacitors simulated by standard capacitor model.

For more general modelling (including large-signal behavior) by pointwise linearization, the functional relationship is not known in general but can be approximated emipriically for a given device by measurements, if the desired degree of accuracy so required.

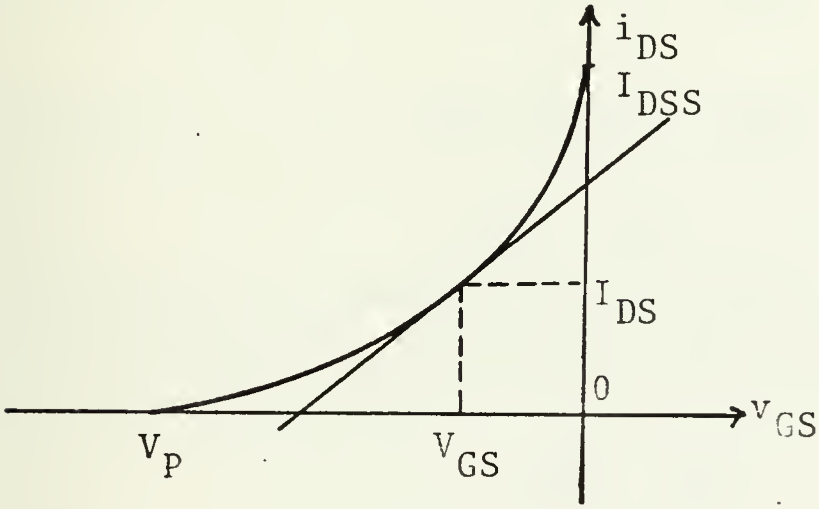


Figure 4-19. Pinch-off Region Transfer Curve Showing Pointwise Linearization Procedure

Transconductance g_m is the slope of the transfer characteristic curve, Fig. 4-19. At a point (V_{GS}, I_{DS}) the tangent line is given by

$$i_{DS} = g_m (v_{GS} - V_{GS}) + I_{DS} \qquad 4.43$$

where

$$g_m = (-2\ I_{DSS}/V_P)[1 - (V_{GS}/V_P)] .$$

I_{DS} in the pinch-off region is expressed as in Eq. 4.44.

$$I_{DS} = I_{DSS}[1 - (V_{GS}/V_P)]^n \qquad 4.44$$

where n is a constant for a given unit, whose value usually lies between 1.7 and 2.7 (for many units n = 2 is a good assumption), and I_{DSS} is the drain current when $v_{GS} = 0$. The determination of the necessary model parameters will be given in the following section.

3. Determination of Model Parameters

Capacitance determination: For the model represented in Section 2, the common-source short-circuit input, output, and reverse capacitances are given in the following expressions, respectively:

$$C_{ISS} = C_{DG} + C_{GS}$$

$$C_{OSS} = C_{DG} + C_{DS}$$

$$C_{RSS} = C_{DG} \quad .$$

Consequently, the model capacitances may be calculated in terms of the short-circuit capacitances as

$$C_{DG} = C_{RSS}$$

$$C_{GS} = C_{ISS} - C_{RSS} \quad .$$

$$C_{DS} = C_{OSS} - C_{RSS} \quad .$$

If the capacitances C_{ISS}, C_{OSS}, and C_{RSS} are not supplied by the manufacturer the following measurement method can be used to determine the unknown values. Three terminal instruments are the most useful, since in addition to measuring the capacitance between two terminals, they are equipped to eliminate the effects of capacitance between these two terminals and a third terminal. This is shown in Fig. 4-20. In Fig. 4-20 the presence of C_1 and C_2 does not affect the measurement of C_x. In some instruments the "low" terminal is grounded and the terminal connected to both C_1 and C_2 is called the "guard" terminal. Capacitance measurement jigs

are diagramed in Fig. 4-21. The limitations on this measurement are: (1) the gate signal should usually be limited to less than 200 mV, (2) frequency should be kept between 500 KHz and 5 MHz. Below 500 KHz the chokes must be large, and above 5 MHz series resonance and some other detrimental effects occur.

Conductance Measurement: The pinch-off voltage, V_p, the drain saturation current, I_{DSS}, the drain conductance, g_D, and the transconductance g_m are four of the parameters required in the models presented in this section. For the pinch-off region, the transconductance is given by Eq. 4.45.

$$g_m = (-2I_{DSS}/V_P)[1 - (V_{GS}/V_P)] \qquad 4.45$$

if $V_{GS} = 0$ then g_m is maximum,

$$g_{max} = -2\ I_{DSS}/V_P$$

or

$$V_P = -2\ I_{DSS}/g_{max}\ .$$

The experimental circuit for determination of g_{max} is given in Fig. 4-22.

The determination of g_D can be done by a circuit as shown in Fig. 4-23, in which g_D(micromho) = 100 V_2(mV) when V_1 = 1.0 volt.

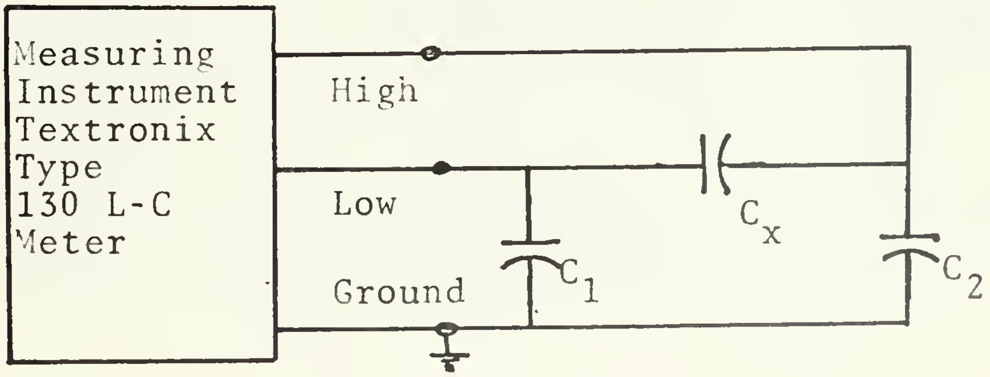
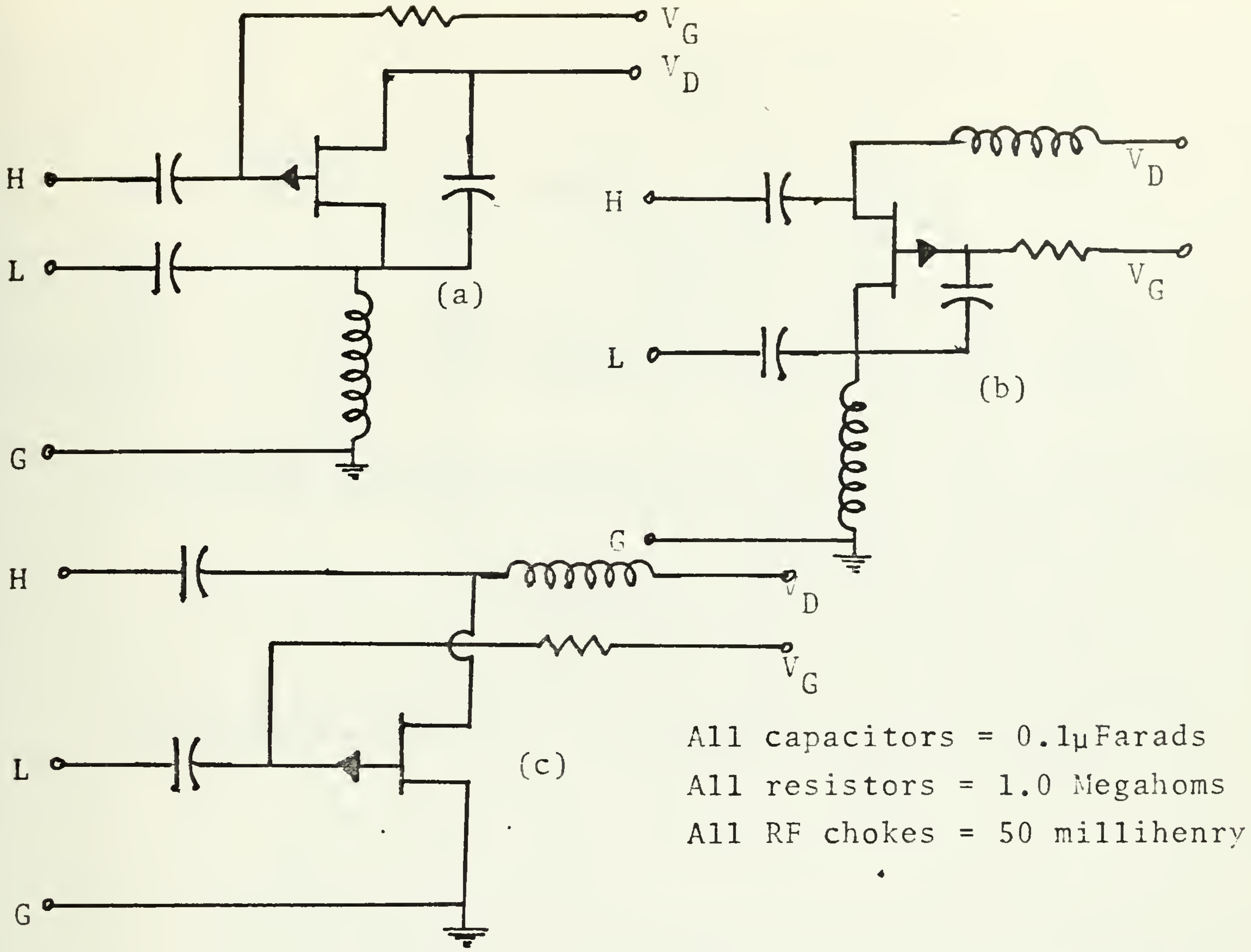


Figure 4-20. Three Terminal Measurement



All capacitors = 0.1μFarads
All resistors = 1.0 Megahoms
All RF chokes = 50 millihenry

Figure 4-21. (a) C_{ISS} Measurement, (b) C_{OSS} Measurement, (c) C_{RSS} Measurement Jigs

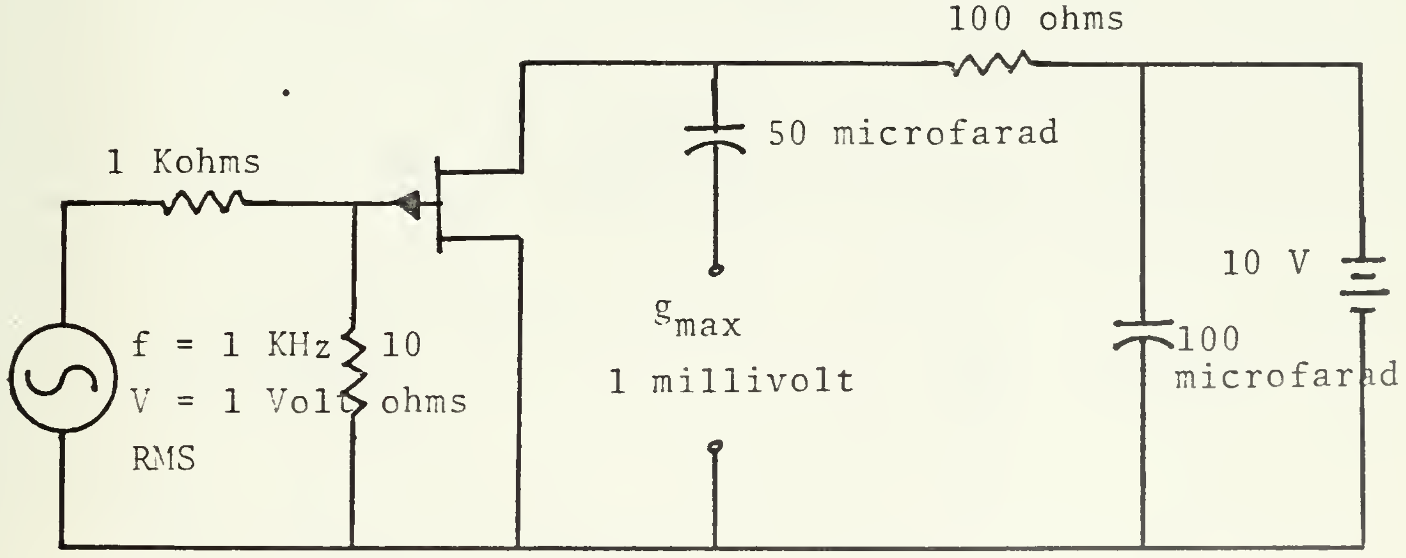


Figure 4.22. Circuit for measurement of g_{max}

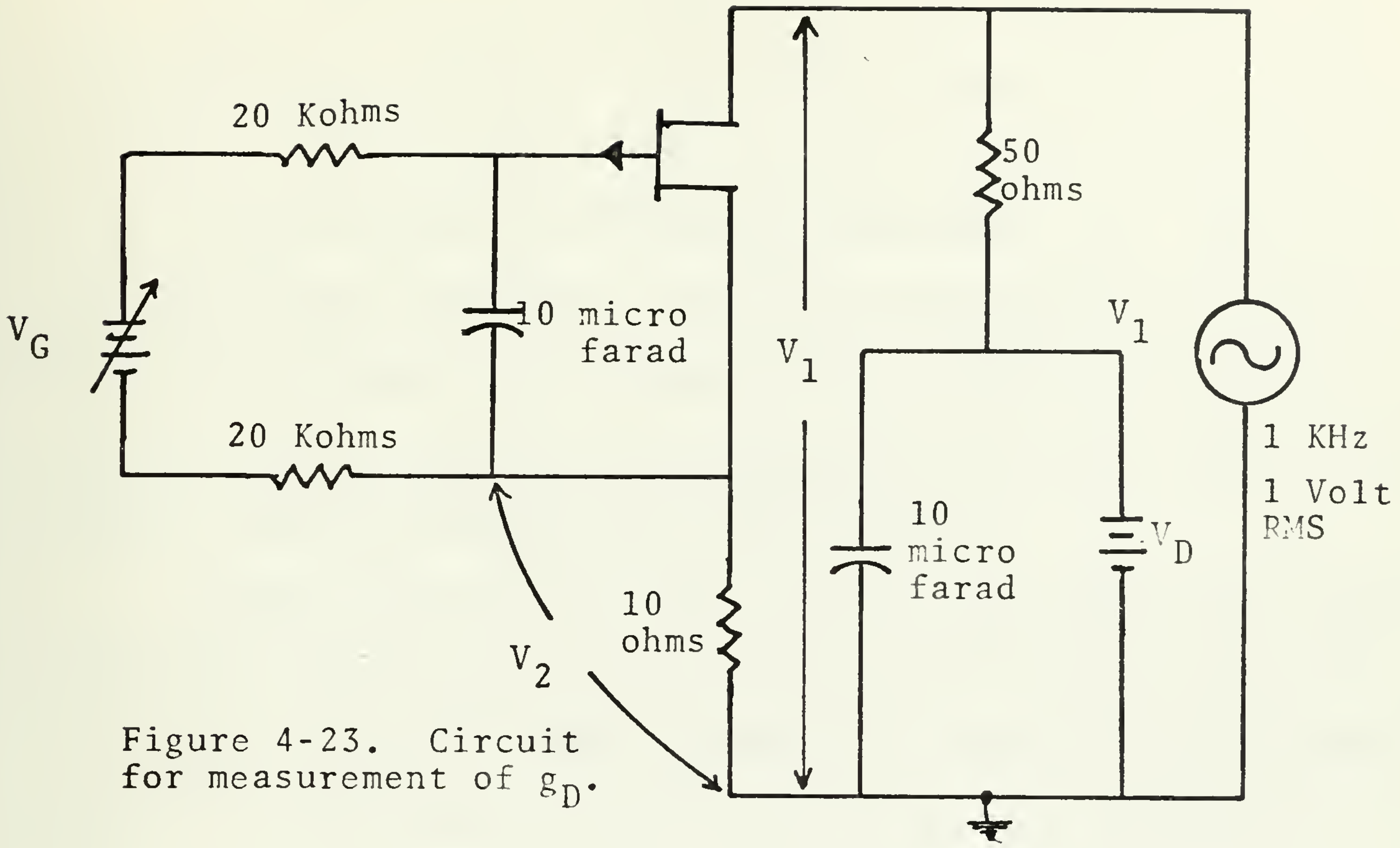


Figure 4-23. Circuit for measurement of g_D.

Current Measurement:

I_{DSS} is the easiest determined parameter as far as the measuring circuit is concerned. The following configuration can be set for determination of I_{DSS}.

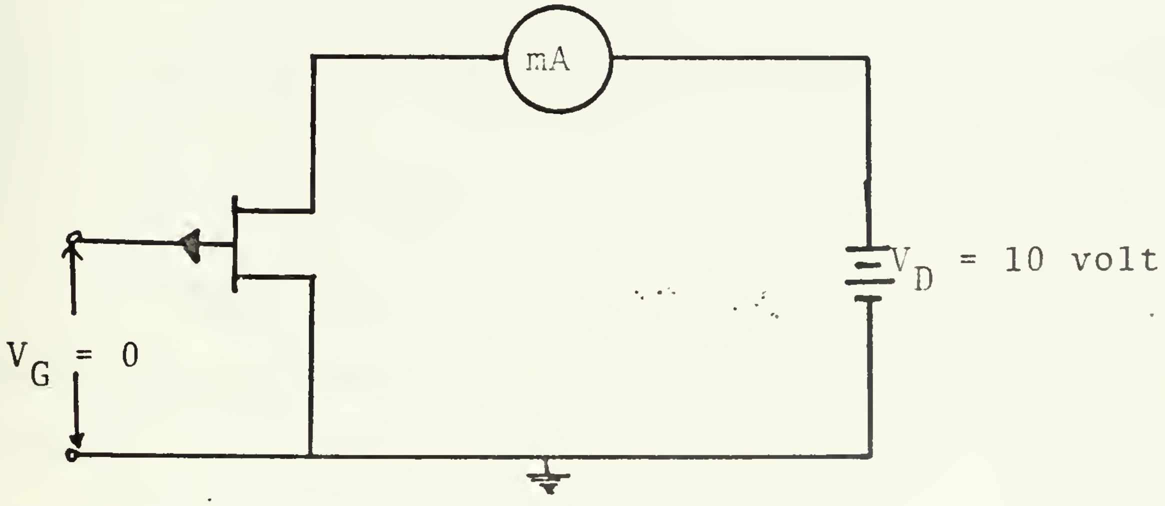


Figure 4-24. Circuit for Measurement of I_{DSS}

4. Modified Model

As pointed out in Chapter III, the major effects of temperature on a FET are to alter the average channel conductivity, σ, and the gate-channel junction barrier potential, ψ. Since σ decreases with increasing temperature, the effect of this to decrease the drain current as the temperature rises. On the other hand, $|\psi|$ decreases with increasing temperature, causing the magnitude of the total gate-source potential to be reduced, hence increasing the drain current.

Next, consider the three terminal FET to be operated in the saturation region with a constant gate-source emf. Therefore, $I_{DS} = I_{DS}(\psi,\sigma)$. The differential equation for the drain current is given [Ref. 8] by the following relationship:

$$dI_{DS}/dT = (\partial I_{DS}/\partial\psi)(d\psi/dT) + (\partial I_{DS}/\partial\sigma)(d\sigma/dT)$$

$$= g_m\,(d\psi/dT) + (I_{DS}/\sigma)(d\sigma/dT) \qquad 4.46$$

since $\partial I_{DS}/\partial\psi = g_m$ and I_{DS} is proportional to σ at a given temperature T. A reasonable approximation to the mobility-temperature function [Ref. 2] is

$$\mu = \mu_o(T/T_o)^{-n}$$

where n depends on the impurity concentration. Therefore, after necessary manipulation the following equation is obtained:

$$(1/\sigma)(d\sigma/dT) = -n/T \qquad 4.47$$

If $\Delta T \ll T$ then $d\psi/dT$ can be approximated by ±2.2 mV/°C (depending upon whether the transistor is p-channel or n-channel, respectively) at low source current level. For many purposes n may be approximated to 2 (actually it ranges from 1.7 to

2.7). Taking the above approximations into account the Eq. 4.48 can be obtained for drain current change with respect to temperature.

$$dI_{DS}/dT \cong 2.2(\text{mV}/°\text{C})\ g_m - n\ I_{DS}/T \qquad 4.48$$

It is easily seen from Eq. 4.48 that the condition for zero temperature coefficient is approximately given by

$$I_{DS}/g_m \cong 2.2(T/n)\ \text{mV}\ . \qquad 4.49$$

When the change in temperature is very small compared to the given temperature, T ($\Delta T << T$), Eq. 4.48 can be expressed in the following form:

$$\Delta I_{DS}/\Delta T \cong 2.2(\text{mV}/°\text{C})\ g_m - n\ I_{DS}/T$$

then

$$\Delta I_{DS} \cong 2.2\ g_m\ (\Delta T) - (n/T)\ I_{DS}(\Delta T)\ . \qquad 4.50$$

Therefore, one may represent Eq. 4.50 using two current generators with current directions opposing to each other. Applying the Eq. 4.50 to Fig. 4-17 the FET computer model is obtained for a given temperature T and the temperature change $\Delta T << T$, as shown in Fig. 4-25. If ΔT is large, one has to make iterative computations by taking proper ΔT increments.

The necessary model parameters may be determined as explained in the previous section. The currents I_1 and I_2 caused by the temperature can be expressed in terms of known parameters as

$$I_1 = 2.2\ g_m\ (\Delta T) \qquad 4.51$$

$$I_2 = (n/T)\ I_{DS}\ (\Delta T) \qquad 4.52$$

To be dimensionally correct g_m should be in millimhos, temperature T and (ΔT) in degrees Kelvin.

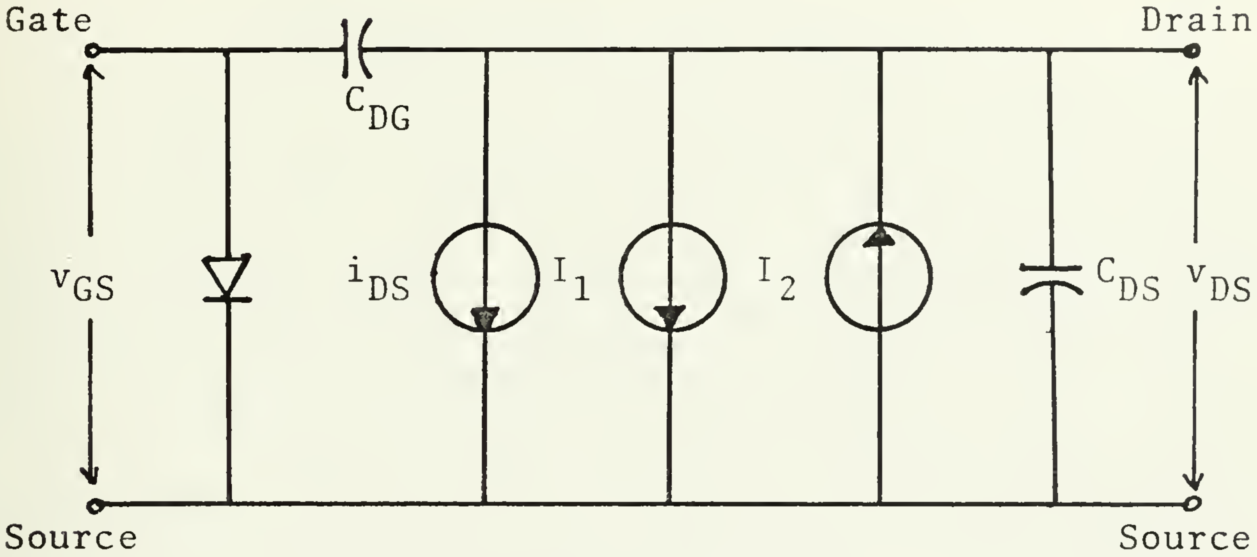


Figure 4-25. Lumped JFET Computer Model with Temperature Effect.

The enhancement-type MOSFET has a characteristic threshold voltage, V_T, instead of the pinch-off voltage, V_P, but the equations are of the same general form: for $0 < v_{GS} - V_T < V_{DS}$ (pinch-off region) $i_{DS} = K(v_{GS} - V_T)^2$. Here K is a constant and is a function of channel geometry, doping, and effective carrier mobility. In this section an analysis is given for the temperature dependence of v_{GS} when the current is maintained constant and saturation conditions are present. It is assumed that interface charge Q_{SS} is independent of temperature and that the effects of a finite drain resistance can be neglected. Further, it is assumed that the only temperature dependent quantities are v_{GS} (DC gate-source voltage), ϕ_F (Fermi potential) and μ_n (effective

surface mobility). The temperature coefficient as a function of v_{GS} is given [Ref. 8] by

$$dv_{GS}/dt = (i_D/g_m)(-1/\mu_n)(d\mu_n/dT) - (d\phi_F/dT)\{[-2(v_{GS} - V_T)/v_{DS}] + 1\} \qquad 4.53$$

Since the first and the second terms are both positive, it is evident that there may exist a realizable zero temperature coefficient point. Supposing that the mobility is proportional to $T^{-1.5}$ and letting n = 2, one can obtain (by taking certain known factors and coefficients into account) the following expression for temperature coefficient [Ref. 8].

$$dv_{GS}/dt = (3.0/T)(v_{GS} - V_T) - [(0.605 - \phi_F)/T]\{[2(v_{GS} - V_T)/v_{DS}] - 1\} . \qquad 4.54$$

As pointed out by Giralt et al. [Ref. 23], 'a good approximation to the behavior is given by

$$d|v_{GS}|/dT = h - 2.5|v_{GS} - V_T| \text{mV/°C} \quad , \qquad 4.55$$

where V_T is the measured threshold voltage obtained from the straight line extrapolation of an I_D/g_m plot on the v_{GS} axis, and h is a constant whose value is somewhat dependent on the subsrate doping but normally lies between 2 and 6.

If $\Delta T << T$ then the Eq. 4.55 can be written as in Eq. 4.56.

$$\Delta|v_{GS}| = h(\Delta T) - 2.5|v_{GS} - V_T|(\Delta T)\text{mV} . \qquad 4.56$$

On the other hand when temperature changes as much as ΔT Eq. 4.43 becomes

$$i_{DST} = g_m[(v_{GS} + |\Delta v_{GS}|) - V_{GS}] + I_{DS}$$

$$= g_m\ v_{GS} + g_m|\Delta v_{GS}| - g_m\ V_{GS} + I_{DS}$$

$$= i_{DS} + g_m|\Delta v_{GS}| \quad . \qquad 4.57$$

This change Δv_{GS} can be obtained either from Eq. 4.54 or Eq. 4.56 depending upon the given (or known) information. The term ($g_m|\Delta v_{GS}|$) can be defined as temperature resultant current generator than temperature dependent computer model for MOSFET obtained as shown in Fig. 4-26.

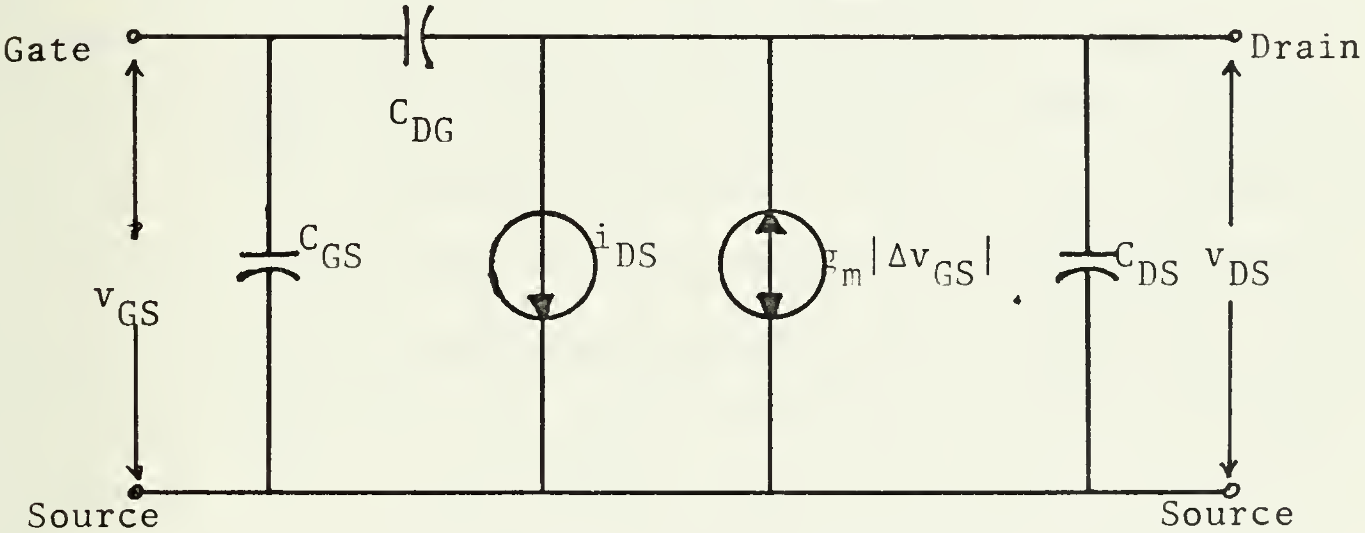


Figure 4-26. Lumped MOSFET Computer Model with Temperature Effect

V. CONCLUSIONS

A. GENERAL

It has been shown that temperature variations have various effects on different electronic components. Resistance of a resistor increases or decreases with temperature depending on the material used. Inductance of an inductor may or may not change with temperature depending on its physical dimensions and the material used. Capacitance of a capacitor changes slightly with temperature. However, this small change can be extremely important in some situations (e.g., as in resonance circuits). Forward diode currents and diffusion capacitance increase with increasing temperature. The effect on a transistor is quite complex, and some simplifying assumptions are listed in Chapter IV. The junction forward current and diffusion capacitance increased with increasing temperature. Reverse saturation current also increased. Two types of field-effect transistors were examined separately. It was found that with the proper operating point, the temperature effect could be eliminated. If this operating point cannot be attained, the drain current changes. Therefore, the effects discussed above should be applied to the computer models when one attempts to analyze a circuit which is composed of electronic components.

The models proposed here allow simulation of the behavior of several circuit components. For a reasonably accurate

simulation, the parameters required for the models were few easily determined. The actual circuit in which the component is to be used is a major factor in the choice of a model and the use of these models must be done with an understanding of the assumed operating regions and characteristics of the components themselves. The parameters of the model must also be chosen to suit the particular application, because even the best models can only approximate the behavior of the actual devices.

Emphasis was placed on empirical determination of parameters; however, these parameters may also be determined from the material characteristics and structural geometry of the devices being modelled.

These models are useful in analysis and design of electronic circuits. Also, since the model parameters may be calculated from information on the construction of the device, it should be possible to predict the behavior of a type of component before it is fabricated.

The models are general so that they are compatible with most of the electronic circuit analysis programs in use today.

B. SUGGESTIONS FOR FURTHER STUDY

1. Modification of Models with High Frequency Effects

High-frequency models for the components are more complex than low frequency models, since additional reactive elements must be included. As a suggestion for further study, one might consider the effects of high frequency effects

upon these components under normal operating temperatures and temperature as a variable.

2. FET in Triode Region

As far as the FET is concerned, the developments were done for the saturation region operation. The other very important application is the triode-region operation. In triode region, $(0 < v_{DS} \ll v_{GS} - V_P)$ the g_{DS} is expressed as

$$g_{DS} = (I_{DSS}/V_P^2)[2(v_{GS} - V_P) - 2v_{DS}] \, . \qquad 5.1$$

At an arbitrary point (V_{DS}, I_{DS}) on the output characteristic curves, the pointwise linear approximation to the output curve is the straight line $i_{DS} = g_{DS}\,(v_{DS} - V_{DS}) + I_{DS}$ where g_{DS} is the slope at (V_{DS}, I_{DS}) given with Eq. 5.1. Then it should be simple to develop models for triode region for various FET's by taking the temperature effects into account.

3. Some Other Device Models

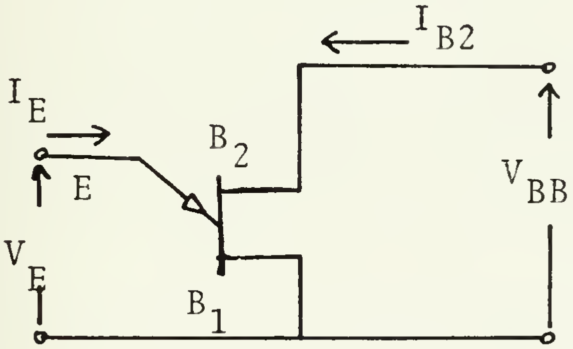
One might also develop computer models for additional devices depending upon the methods stated in this paper with temperature or high frequency effects in mind.

(a) Zener/avalanche diode model: Since the avalanche diode is nearly identical to an ordinary diode for operating voltages greater than V_B (breakdown voltage), it should be possible to modify the Fig. 4-9, diode computer model to include the avalanche phenomenon.

(b) Tunnel diode model: The unique properties of tunnel diodes which are most often utilized are its negative

resistance and its very rapid switching from V_p (peak voltage) to a point in the forward conduction region. Most tunnel diode circuits are designed around the peak point and valley point. Any tunnel diode model should accurately approximate these points as well as modelling other important properties. It is relatively easy to measure the peak point, valley point and the maximum slope in the negative conductance region. There is very little resistance to current flow when reverse bias is applied to the junctions; i.e., with reverse bias, the tunnel diode is nearly a short circuit.

(c) Unijunction transistor: On the emitter characteristics the peak point is defined by the expression $V_p = v + aV_{BB}$ where v is defined by the $I_{B2} = 0$ curve. The quantity a, called the intrinsic standoff ratio. When I_E becomes greater than I_p (peak point current), the process of conductivity modulation occurs in the semiconductor material between emitter and base-1, causing the negative resistance characteristic. As I_E is increased well beyond I_p there is also a slight conductivity modulation of the B_1 - B_2 region resulting in an increased I_{B2}. A model which will adequately describe the static behavior of a unijunction transistor can be formulated.



(3) Silicon controlled rectifiers: Since silicon control rectifier (SCR) is a four-layer, three-junction device with only three leads, it is difficult to describe the internal behavior. The two-transistor analogy provides a good intuitive feel for the operation, but it is difficult to obtain the transistor parameters since base-1 and collector-2 are not accessible. It should be possible to represent an SCR by empirically relating the internal behavior to terminal characteristics even the physical processes are somewhat more complex than for some of the devices discussed previously.

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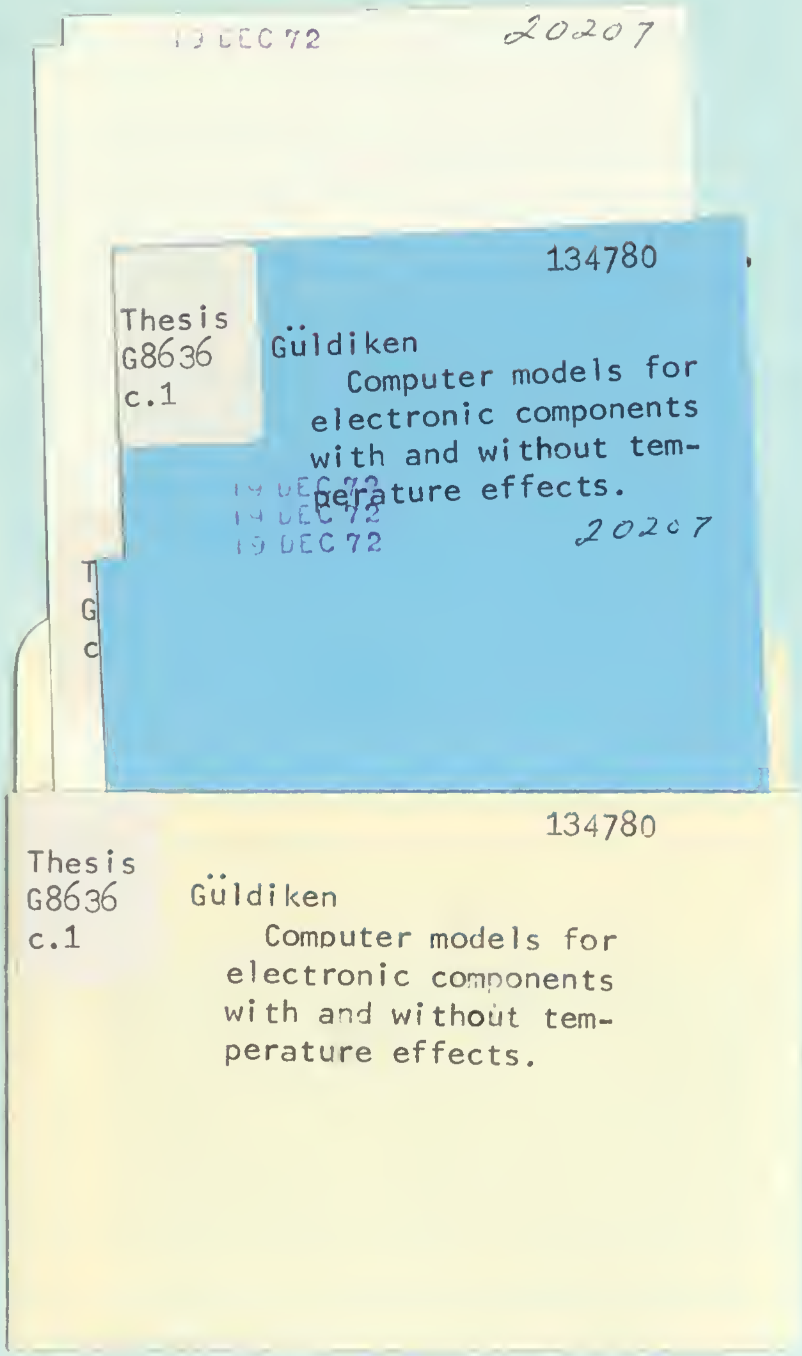
13. ABSTRACT

Whenever active or passive devices are included in an electronic circuit that is to be analyzed by a computer, appropriate models for these devices must be developed. The majority of the models that have been adapted for analyzing a circuit on a computer have neglected the effect of ambient temperature on the element. Temperature variation has been shown to have hazardous effects on electronic components. This paper deals with the modification of some existing models to include temperature effects and shows the results of such modifications. It is done for six basic electronic components (i.e., resistor, capacitor, inductor, diode, bipolar transistor and field-effect transistor). Suggestions for extension of this work are also included.

KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Computer Models						
Temperature Effects						
MOSFET						
JFET						
Transistor						



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